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An Efficient Accuracy Switchable Majority Based Prefix Adder

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Abstract : Parallel-prefix adders offer a highly efficient solution to the binary addition problem and are well suited for VLSI implementations. Approximate computing allows to improve latency, area, or power consumption for the sake of accuracy. This means that an error in computation may be tolerated as long as it is small enough to maintain a feasible operation of the system.In this work we propose a majority based prefix adder able switching between both exact and inexact mode .the structure more area and delay efficient than existing approximate adders by some modifications in carry calculation stage .proposed structure has been coded in HDL and implemented in vertex FPGA.

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