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Investigation of Dual Bridge Multilevel DC Link Inverter for PV Application

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Abstract : The main objectiveof the proposed topology is to synthesize a high quality sinusoidal output voltage with considerably reduced switch count than the conventional MLI. The proposed topology consist of series connected H-bridge and diodes. The number of levels dependson dc source arrangement. Heredc sources can be replaced by PV.The proposed PV based dual bridge MLDCLI (DBMLDCLI) is evaluated using phase disposition (PD) multi-carrier pulse width modulation (MC-PWM) strategy.The performance of a dual bridge dc-link inverter topology is simulated through MATLAB/SIMULINK and the THD of the output voltage is analyzed. The results are validated.
Keywords : Dual Bridge Multilevel Dc Link Inverter (DBMLDCLI), Phase Disposition (PD), THD

Introduction

MLIs are preferred for high power medium voltage applicationsdue to their donation of reduced harmonic content in the output side, lower blocking voltage in the switching devices[1,2].but it requires large number of semiconductor switches, each switch requires a related gate driver circuits which are more expensive and complex[3-6],these demerits are eliminated by the topology called multilevel dc link inverter which gives improved performance. These inverter reduce the number of switches and gate drive as the number of voltage levels increases. However it shows inconveniences in their operation with balancing capacitor voltage[7-9]. Therefore proposed topology PV based Dual Bridge Multilevel DC link Inverter (DBMLDCLI) which requires a less number of power switches with nearly sinusoidal output voltage. It uses lower number of sources, power switches and eliminates the necessity of capacitors. This paper presents dual bridge 15 level inverter with phase disposition(PD) multi-carrier pulse width modulation(MC-PWM) technique which is used forcontrol the switches of inverter and it is carried out in MATLAB/SIMULINK.

PV Modelling

PV module is used for power conversion. The output characteristics of a PV module depend on the solar irradiance, the cell temperature and the output voltage of the PV module. Equivalent circuit of a PV cell is

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shown in Fig. 1. The simplified equivalent circuit of solar cell consists of diode and current source which are connected in parallel. The current source I_{ph} representthe cell photo current. R_p and $R_s$are the parallel and series resistances of the cell respectively. The output current and voltage from the PV cells are represented by I and V.

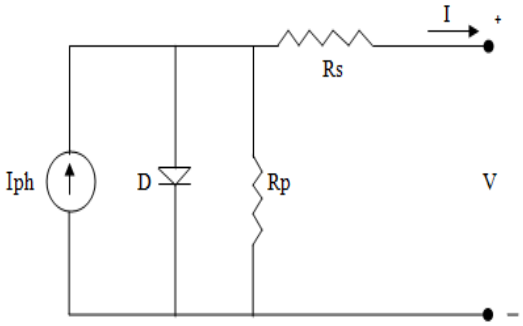

Fig.1 Equivalent circuit of PV

The output currentof PV is given by,

The output current of PV is given by,

$$I = I_{ph} - I_s\left(e^{\frac{q(V+IR_S)}{nkT}} - 1\right) - \frac{V+IR_S}{R_p} \qquad (1)$$

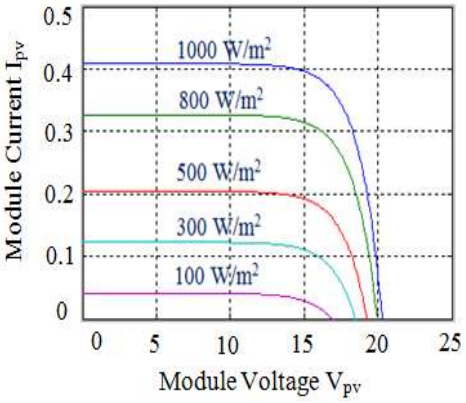

Fig.2 I-V Characteristics of PV module

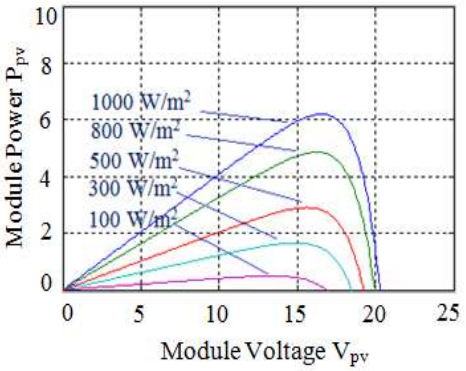

Fig.3 P-V characteristics of PV module

I-V characteristics of PV module for different irradiation are shown in Fig.2 and the P-V characteristics of PV module for different irradiance at 25℃ are shown in Fig.3. Photocurrent depends on the irradiation. The higher the irradiation, the greater the current[10].

Proposed Topology

Fig.4 shows the generalized structure of dual bridge multilevel dc link inverter which is used to realize as many desired levels. It constituted of two H-bridges, PV sources and a number of distinct modules depending on the output voltage level requirements. The first bridge is connected in series with as several modules for every six level increase with each module inter-twined with a switch in series with the source, the combination shunted through an anti paralleldiode. The first H-bridge serve to increase the level of the dc-link voltage, the second H-bridge provides bi-directional power flow through the load[11,12].

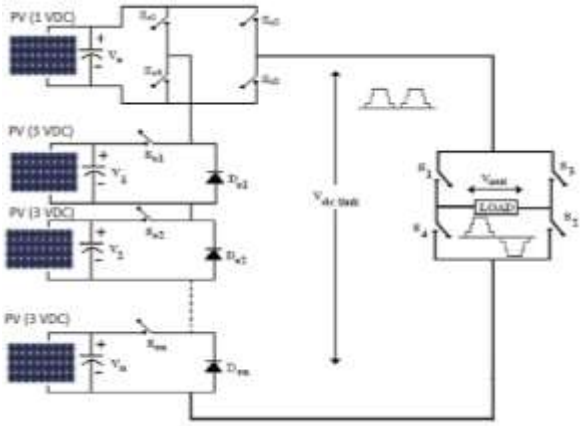

Fig.4 Generalized structure of DBMLDCLI

The defined number of output voltage levels that an new dual bridge dc-link multilevel inverter can synthesize is expressed using a relation (2(3S+1) +1) where S is the number of voltage sources excluding V_0, if arranged in the ratio V_0:V_n = 1:3.

Switching operation: To explain the switching operation for variouslevels, the dc link structure is represented by fixed source. The operation for each level of a fifteen level inverterwith V_0:V_1:V_2 = (4:12:12) V along with positive and negativehalf cycles is explained through switchingtable. It is seenfrom table I that the devices S_{03}, S_{04}, D_{e1} and D_{e2} in the dc-link circuitand either the pair S_1–S_2 or pair S_3–S_4in the H-bridge alternately arerequired to conduct to extract the first level of the output voltageand the second level S_{01},S_{02},D_{e1} and D_{e2} in the dc link circuit and either the pair S_1-S_2 or S_3-S_4 in the H-bridge alternately are required to conduct to extract the second level and so on. Table I. shows switching pattern for proposed dual bridge multilevel dc link inverter.

Table-I switching operation

S_{01}	S_{02}	S_{03}	S_{04}	S_{e1}	S_{e2}	S_1	S_2	S_3	S_4	V_0
0	0	1	1	1	1	1	1	0	0	+7
0	1	0	1	1	1	1	1	0	0	+6
1	1	0	0	1	0	1	1	0	0	+5
0	0	1	1	0	1	1	1	0	0	+4
0	1	0	1	0	1	1	1	0	0	+3
1	1	0	0	0	1	1	1	0	0	+2
0	0	1	1	0	0	1	1	0	0	+1
0	0	0	0	0	0	1	1	0	0	0
0	0	1	1	0	0	0	0	1	1	-1
1	1	0	0	0	1	0	0	1	1	-2
0	1	0	1	0	1	0	0	1	1	-3
0	0	1	1	0	1	0	0	1	1	-4
1	1	0	0	1	0	0	0	1	1	-5
0	1	0	1	1	1	0	0	1	1	-6
0	0	1	1	1	1	0	0	1	1	-7

Control Strategy

In this topology, Phase Disposition (PD) pulse width modulation [13]scheme is used. It is based on a comparison of a sinusoidal reference waveform with vertically shifted carrier waveform generates PWM signals. All the carrier signals have the same amplitude, same frequency and are in phase[14]. The generated seven PWM signals are applied to the switches of H-bridge along with modules to produce dc-link voltage. Common H-bridge used to produce ac output voltage by using reverse voltage technique. ThisPWM method gives rise to the lowest harmonic distortion when compared to other methods [15]. The Fig.12 shows that carrier and reference sinusoidal signals of phase disposition modulation.

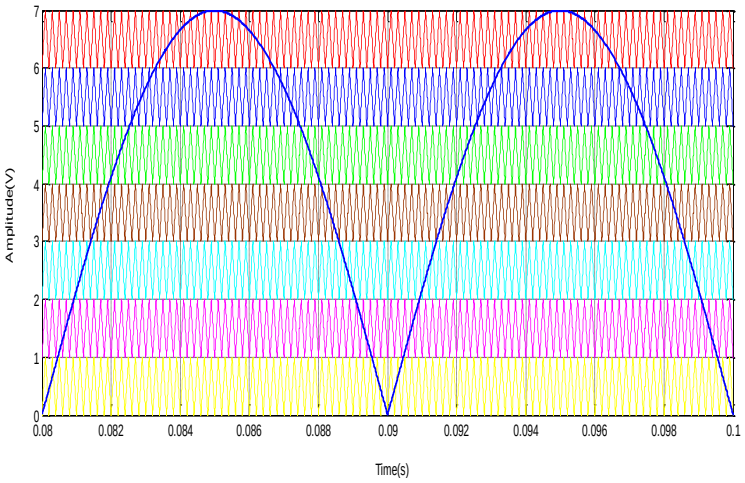

Fig.12The reference and carrier signals of PD PWM technique

Simulation Results

Simulation of the circuit is carried out inMATLAB/SIMULINK. Fig.13 shows the simulation diagram of fifteen level DBMLDCLI. The PV sources are chosen in the ratio 1:3 (V_1 = 4 V, V_2 = V_3 = 12 V) withR load of 100Ω. It uses a PD-MC-PWM technique with a carrier frequency of 5 kHz. Gating pulses for the switches are shown in fig.14. The multilevel dc-link voltage obtained through first H-bridge with distinctive module is shown in Fig.15. Fig.16. shows the output voltage waveform of fifteen level dual bridge multilevel dc link inverter which is obtained through second H-bridge and the FFT analysis of voltage total harmonic distortion is depicted in Fig.17.

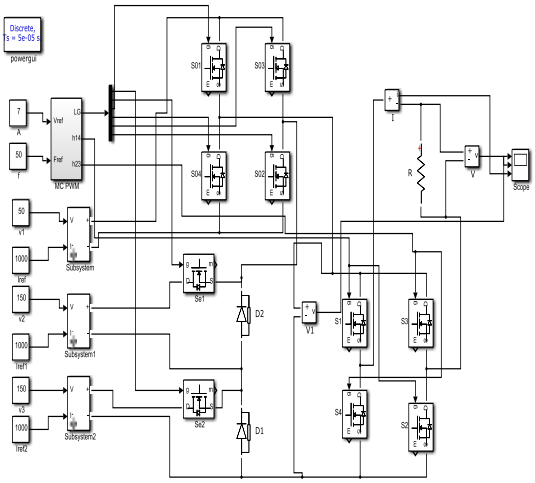

Fig.13 Simulation diagram of 15-level DBMLDCLI.

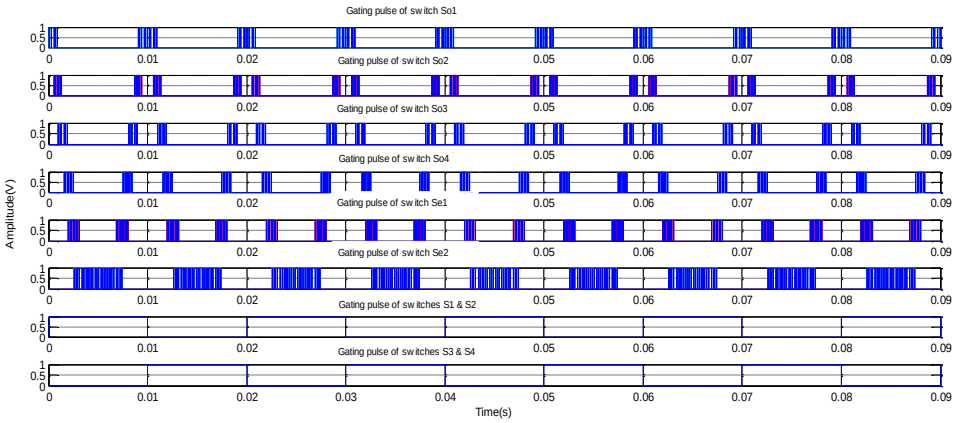

Fig.14 Pulse pattern

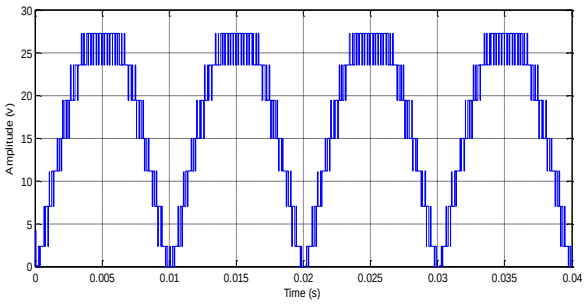

Fig.15 DC Link Voltage Waveform

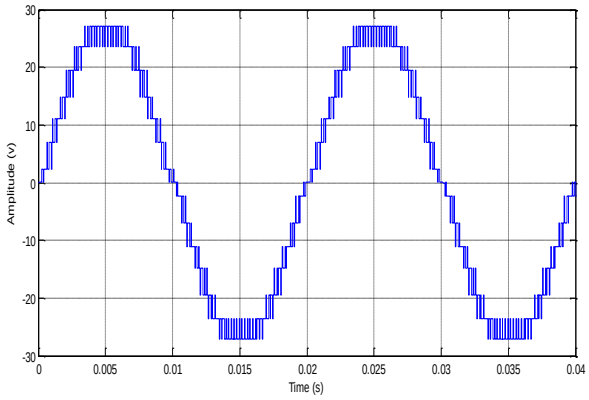

Fig.16Output Voltage Waveform of 15-level DBMLDCLI

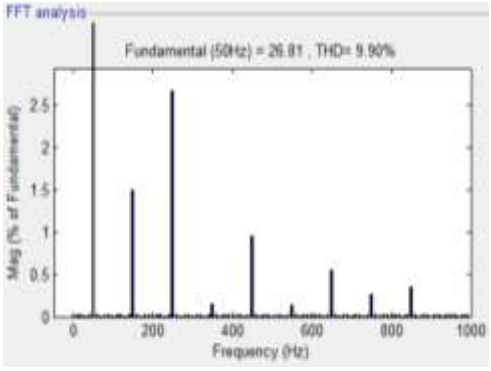

Fig.17 Harmonic Spectrum of Output Voltage

A detailed comparison of the switch and source requirements is tabulated in Table II to bring out the reduction in the switch count of the proposed DBMLDCLI over the existing MLI topologies for a typical case of fifteen level output. From table II it is observed that conventional topologies switch count increased by 55% than proposed topology.

Table II Comparison between topologies for fifteen level.

Multilevel inverter structure	**Multilevel DC link Inverter**			**Proposed topology**
	Cascaded half bridge	**Diode clamped**	**Flying capacitor**	
Main switches	18	18	18	10
Bypass diodes	-	-	-	2
Clamping diodes	-	12	-	-
DC split capacitors	-	6	6	-
Clamping capacitors	-	-	6	-
Dc sources	7	1	1	3
Total	25	37	31	15

Hardware Implementation

The hardware layout of the system is shown in fig.18. The inverter was constructed using IRF640 MOSFET switches. The inverter is also interfaced with the PV system. The voltage generated from the solar panel given to the inverter are V_1=4V,V_2=12V and V_3=12V.

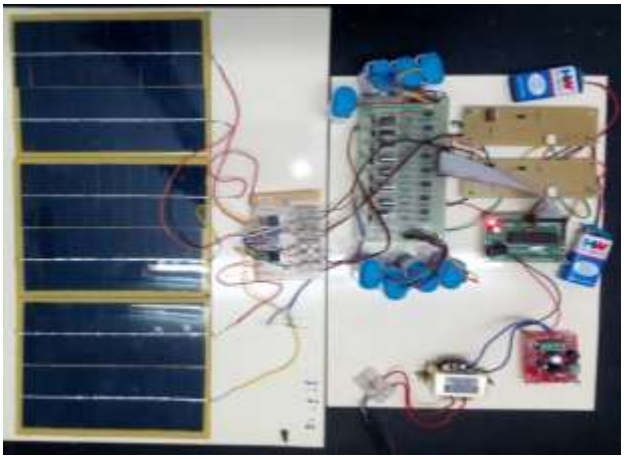

Fig.18 Hardware Circuit

The gating signals for the multilevel inverter are implemented using microcontroller ATMEGA8. Fig.19(i)- 19(x) shows the switching pulses generated for each MOSFET switch where they are given to the gate terminal of the MOSFET switch in the inverter.

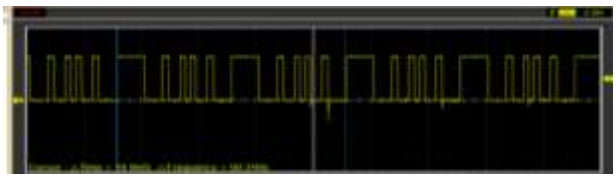

Fig.19 (i) Gating pulse of switch S_1

Fig.19 (ii) Gating pulse of switch S_2

Fig.19 (iii) Gating pulse of switch S_3

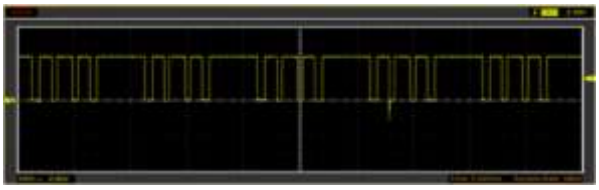

Fig.19 (iv) Gating pulse of switch S_4

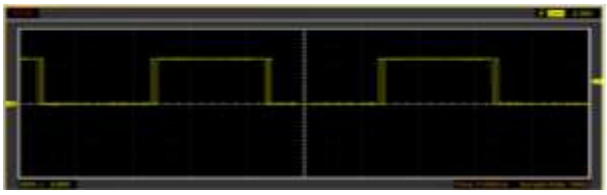

Fig.19 (v) Gating pulse of switch S_5

Fig.19 (vi) Gating pulse of switch S_6

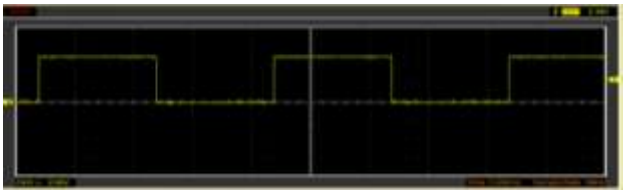

Fig.19 (vii) Gating pulse of switch S_7

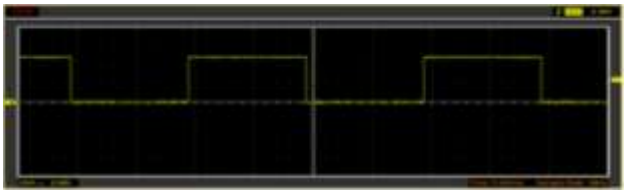

Fig.19 (viii) Gating pulse of switch S_8

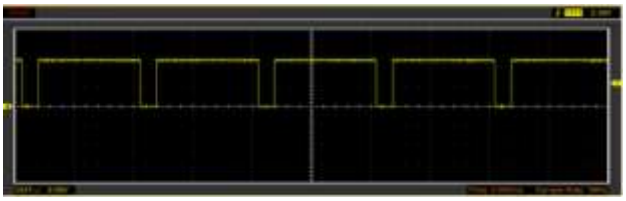

Fig.19 (ix) Gating pulse of switch S_9

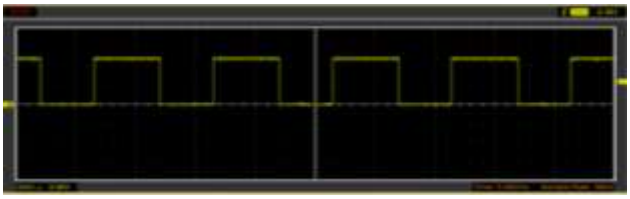

Fig.19(x) Gating pulse of switch S_{10}

Fig.19 Switching Pulse pattern

Fig.20,21 shows dc link voltage and load voltage of DBMLI for dc input voltage (V_1=4V,V_2=12V,V_3=12V) and ac RMSoutput obtained from R load is 26.81V.

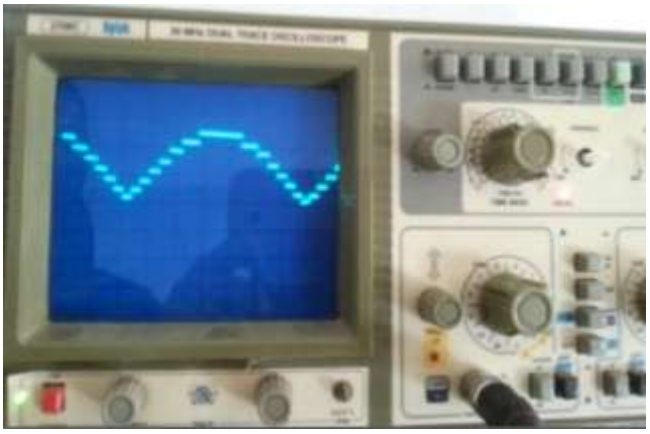

Fig.20 DC Link Voltage Waveform

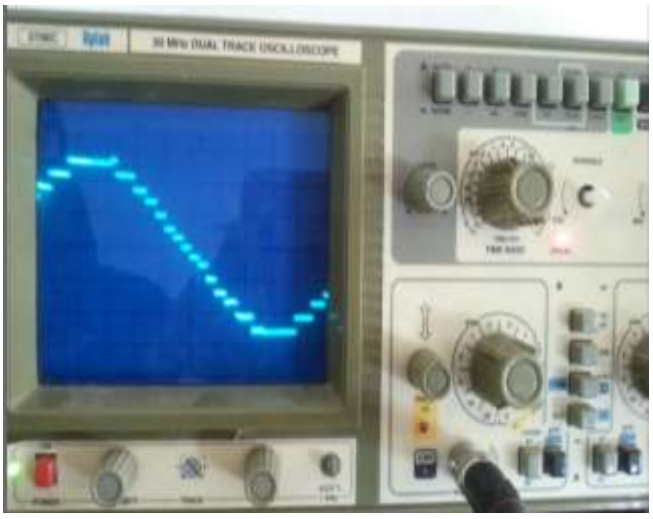

Fig.21 Output voltage waveform of 15-level DBMLDCLI

VI. Conclusion

In this paper, fifteen level PV based dual bridge DC-link inverter topology is proposed with PD PWM technique and it is simulated with MATLAB/SIMULINK.The complete hardware of fifteen level dual bridge dc link inverter is implemented. The obtained result gives reduced voltage THD of 9.9% .Compared to conventional MLI, proposed topology gives better sinusoidal 15-levels of output voltage with lowest switch count.

References

1. Lai Jih-Sheng and Peng Fang Zheng.Multilevel converters - a new breed of power converters.IEEE Trans IndAppl 1996;32:509-17.
2. Rodriguez J, LaJih-Sheng, Peng Fang Zheng.Multilevel inverters: a survey of topologies, controls, and applications IEEE Trans IndElectron2002;49:724–38.
3. Marchesoni M, TencaP.Diode- clamped multilevel converters: a practicable way to balance dc-link voltages.IEEE Trans Ind Electron 2002;49:752–65.
4. Escalante MF, Vannier JC, Arzande.A flying capacitor multilevel inverters and DTC motor drive applications.IEEE Trans Ind Electron 2002;49:809–15.
5. Kouro S, et al. Recent advances and industrial applications of multilevel converters.IEEE Trans Ind Electron 2010;57:2553–80.
6. FangZhengPeng, Jih-Sheng Lai, et al. A multilevel voltage - source converter system with balanced Dc voltages. In: Proceedings of IEEEinternational conference, vol. 2; 1995. p. 1144 –50.
7. Ramkumar S, Kamaraj V, Thamizharasan S, JeevananthanS.A new series parallel switched multilevel dc-link inverter topology.Int Electric Power Energy Syst 2012;36:93–9.
8. Gui-JiaSu.Multilevel dc-link inverter. IEEE Trans IndAppl 2005; 41: 848–54.
9. Vivek Kumar Singh, Praveen Bansal .Asymmetrical 9-level Dual Bridge DC-Link Inverter Topology.International Journal of Electronics, Electrical and Computational System (IJEECS) Volume 4, Special Issue May 2015.
10. RamosHermanz JA, Campayo Martin JJ, et al. Modeling of photovoltaic module.International Conference on Renewable Energiesand Power Quality (ICREPQ'10), Granada (Spain).
11. Manjunatha YR, AnandBA.MultilevelDC Link Inverter with Reduced Switches and Batteries. International Journal of Power Electronics and Drive System (IJPEDS) Vol. 4, No. 3, September 2014, pp. 299-307.
12. MadhuSagarbabu G, Durga Prasad G and JagathesanV. Multilevel DC-link Inverter Topology with Less Number of Switches. Advance inElectronic and Electric Engineering, Vol 4, No.1 (2014), pp. 67-72.
13. Gomathi C, et al. Comparison of PWM methods for Multilevel inverter.International Journal of Advanced Research in Electrical, Electronics and instrumentation Engineering. vol.2, issue 12, Dec 2013.
14. Mohan D, SreejithB.Kurub.A comparative analysis of multi carrier SPWM control strategies using fifteen level cascaded H-bridge multilevel inverter. International Journal of computer applications. Vol.41-No.21,March 2012.
15. Sangeetha R Gupta, Anitha GS.PD-PWM based cascaded H-bridge multilevel inverter for photovoltaic systems. International Journal of Advanced Research in Electrical, Electronics and instrumentation Engineering. vol.4, issue 7, july 2015.

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