International Journal of ChemTech Research
CODEN (USA): IJCRGG, ISSN: 0974-4290, ISSN(Online):2455-9555
Vol.11 No.04, pp 116-120, 2018

A Novel DBB (Difference Based Borrow) Subtractor for Low Power Applications

Shabeerkhan .S*, Padma .A

CSE, Muthayammal Engineering College, Rasipuram, Namakkal, India

Abstract : Power is one of the most significant design bound after speed, in integrated circuit. One of the basic essential component in such circuit is adder and subtractor. In order to optimize such circuits there is need of designing proficient and low power fundamental blocks. we present a new design of the full subtractor based on difference based borrow calculation . The proposed full subtractor is optimized in terms of delay, cost and power. The proposed reversible full subtractor is shown to be better than the existing design. The proposed subtractors proposed in this work will be useful in a number of digital signal processing applications.

Introduction

A subtractor is one of the important building blocks in the construction of a binary divider. In modern systems, applications are aimed at battery operated devices so that power dissipation becomes one of the primary design restrictions.

In the past processor speed, circuit speed, area, performance, cost and reliability were of prime significance. Power consumption was of secondary concern. However, in recent years power consumption is being given equal significance. The reason for such a changing trend is attributed probably due to the fast increase in portable computing devices and wireless communication systems which demand high speed calculations and complex functionality with low power consumption. In addition to this high performance processors consume severe power which in turn rises the cost associated with packaging and cooling. Afterwards there is a rise in the power density of VLSI chips thereby disturbing the reliability. It has been found that every 10 degree rise in operating temperature roughly doubles the failure rate of components made up of Silicon due to several Silicon failure mechanisms such as thermal runaway, junction diffusion, electro-migration diffusion, electrical parameter shift, package related failure and Silicon interconnect failure. From the environment point of view, the lower the power dissipation of electronic components, lower will be the heat dissipated in rooms which in turn will have a positive impact on the global environment. Also, lower electricity will be consumed.

DOI : http://dx.doi.org/10.20902/IJCTR.2018.110413

Researchers have addressed the design of various adders, subtractors, error tolerant subtraction such as in [1], [2], [3], [4], [5], [6]. However, thed esign of binary subtractors has not been adequately referenced in the literature. In [7], Sum Based Adder is proposed, implemented and compared with the basic adder. Public key cryptography is also implemented with the use of sum based adder. It provides the better performance compared to the design with other types of adders. Based on literature made in sum based adder [7], difference based subtractor is proposed in this paper.

In [8],author proposes various imprecise or approximate Full Adder (FA) cells with reduced complexity at the transistor level, and utilize them to design approximate multi-bit adders. Describe design architectures for video and image compression algorithms using the proposed approximate arithmetic units, and evaluate them to demonstrate the efficacy of our approach.

In [9],author proposed low power hybrid 1 bit and 4 bit FA and compared with the different technologies with different parameters(Propagation delay and power dissipation).

In [10], author proposes a designs of 1-bit hybrid alternative full adder using complementary metal-oxide-semiconductor (CMOS) logic, gate diffusion input (GDI) technique, modified GDI and transmission gate logic. Hybrid adder design 1 provided the improved power dissipation compared with earlier hybrid adder reports and hybrid Adder design 2 is better in terms of number of transistors used to realize the adder.

In [11], author proposed a full adder circuit that consumes the lesser power compared to other adder. Author observes that the power has been reduced due to the elimination of the inverter in the proposed design. In [12], author presented a new 13T full adder design based on hybrid – CMOS logic design style. The proposed 13 transistor Hybrid GDI full adder circuits give superior performance in terms of power consumption, propagation delay and Power Delay Product (PDP) than all the reference full adder circuits and the proposed circuits are also free from the voltage degradation problem that existed for the most of the reference circuits.

In [13], author Main objective of this project is to design 1-bit Full Subtractor by using CMOS180nm technology with reduced number of transistors and hence it is efficient in area, speed and power consumption. In [14], author main objective is to design that half subtractor using either of the two adaptive voltage level(AVL) techniques to reduce the sub threshold leakage current which plays a very important role in the reduction of power dissipation.

In [15], author proposes the design of an energy efficient, high speed and low power full subtractor using Gate Diffusion Input (GDI) technique. The entire design has been performed in 150nm technology and on comparison with a full subtractor employing the conventional CMOS transistors, transmission gates and Complementary Pass-Transistor Logic (CPL), respectively it has been found that there is a considerable amount of reduction in Average Power consumption (Pavg), delay time as well as Power Delay Product (PDP).

In [16],authors main aim is to design the low power full subtractor circuit is the increasing circuit's complexity and demand of portable devices. The main objective of the work is to reduce the power of the circuit either by reducing the number of XOR/ XNOR gate or by using P-XOR/ G-XNOR logic gates which consumes less power in comparison with the conventional XOR/ XNOR gates.

In [17], authors develop one bit half subtractor using CMOS 45nm technology with reduced no of transistor and it is efficient in speed, area, and propagation delay and power consumption. To resolve the huge consumption of power is also a challenging task. Using 45nm technology GDI based circuit can be optimized such parameters.In [18], authors proposes CMOS FULL SUBTRACTOR with 32nm technology is having low power dissipation when compared with other technologies.

Experimental

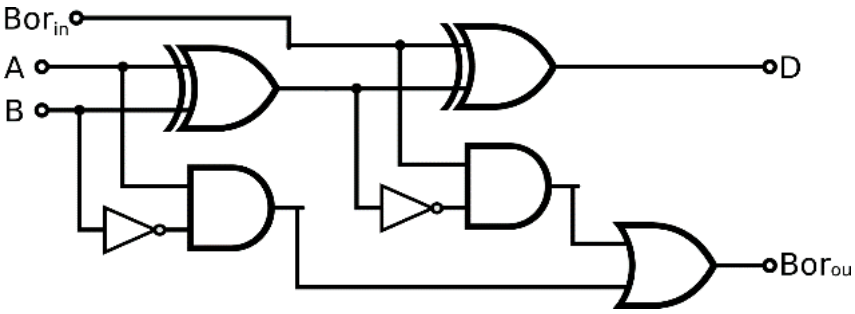

Fig. 1. Conventional Full Subtractor

In normal full subtractor circuit, the outputs are given byD = a ^ b ^ c and Borrow=(~a&.b) +(b&.c) +(c.&~a)So, totally 3 AND gates, 1 three input XOR gate and1 three input OR gate are needed to perform the arithmetic operation and is shown in the Figure 1.In sum based adder Difference D = a ^b ^c and B=~a&c + b &D and is shown in Figure 2 . So, Difference based subtraction operation reduces delay of overall circuit

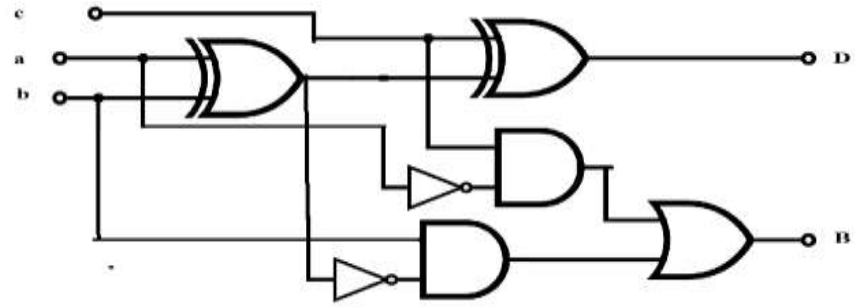

Fig. 2. Proposed Full Subtractor

Result

The conventional and proposed subtractor have been simulated and the parameters such as area overhead, run time and power consumption are compared among them. Based on the performance analysis, it is known that the proposed circuit gives the better results with the reduction of delay overhead and runtime with the considerable reduction in the power consumption. The power consumption have been observed by using the Microwind 3.0 software which uses 0.12 µm technology and its results have been shown in Table 1 and 3. The layout and performance chart has also been shown in 3 & 4.Figure 5 and Figure 6 based on the area overhead and time consumption.

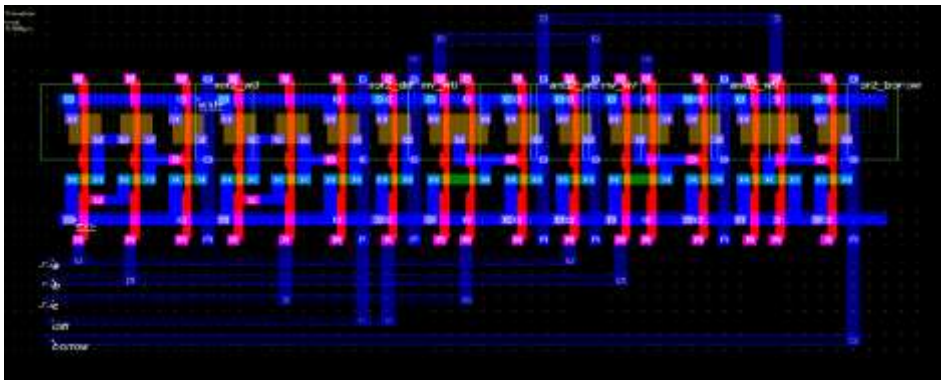

Fig. 3 Layout of Proposed 4 bit Subtractor

Table 1. Delay in ns

Bit size	**1bit**	**4bits**	**8bits**
Conventional	3.057	8	15.06
Proposed	2.89	4.038	8.8

Table 2 Power Results

Bit size	1bit	4bits	8bits
Conventional power (Mw)	9.78 (mW)	0.25(mW)	0.32(mW)
Proposed power (UW)	9.25(uW)	40.8(uW)	72.7(uW)

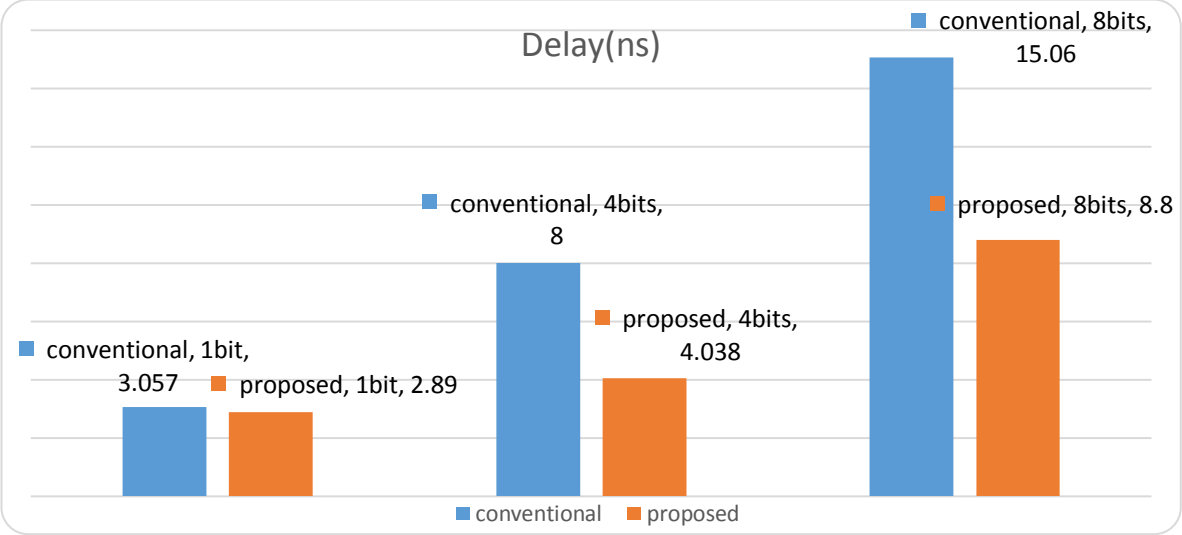

Fig. 4. Performance chart

Discussion

Power and Area are the foremost parameters while designing any VLSI circuits In this work, we have presented efficient designs of full subtractors based on difference based borrow calculation for various bit size. The proposed designs are shown to be better than the existing designs in terms of the delay and power. The proposed efficient designs of subtractors will find applications in emerging vlsi technologies requiring dedicated subtractors units.

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