International Journal of ChemTech Research
CODEN (USA): IJCRGG, ISSN: 0974-4290, ISSN(Online):2455-9555
Vol.11 No.04, pp 38-45, 2018

Modified High Static Gain Single Ended Primary Inductor Converter (SEPIC) For PV Applications

A Kalaivani*, S. K. Nandha Kumar

PSNA College of Engineering & Technology, Dindigul – 624 004, India

Abstract : A novel non-isolated *DC-DC* converter is designed for photovoltaic system is endorsed in this paper. This converter topology is considered by an combination of the classical Boost and SEPIC DC-DC converter. The proposed topology needs only one power semiconductor switch, decreases voltage stress in diodes and power semiconductor switch but also provided that a continuous input current. In addition to that, the topology increasing the voltage static gain while equated with the conventional SEPIC converter. The new converter is integrated with a maximum power point tracking algorithm. Herein, the design considerations of this power converter are presented, and the characteristics of the proposed topology are confirmed by simulations and experiment results.
Keywords : Boost converter; SEPIC converter; photovoltaic; DC-DC conversion.

1. Introduction

DC conversion is of great importance in many applications, starting from low power applications to high power applications. The goal of any system is to emphasize and achieve the efficiency to meet the system needs and requirements. Several topologies have been developed in this area, but all these topologies can be considered as apart or a combination of the basic topologies which are buck, boost and fly-back. Switching regulators use power electronic semiconductor switches in on and off states. switching regulators can achieve high efficiency energy conversion.

The function of a DC-DC converter is to convert a DC input voltage V_s into a DC output voltage V_o. It regulates the DC output voltage against load and line variations. The difficulties occurring regarding the DC-DC converter efficiency is due to the low input voltage, high inrush current and static gain. The boost converter is the conventional non-isolated step up DC-DC converter with limited static gain and high switching voltage stress were used in literature. Most of the high step up converter is affected with high input current because of the inductance Values [1], [12]. To reduce that, the switching frequency has to be increased switches [4]. Moreover, soft-switching is needed to reduce the switching loss and to improve the performance.

Various researchers use the SEPIC converter [2], and the modified SEPIC converter for high static gain applications. The modified SEPIC converter has twice the static gain [6], value when compared with the conventional boost converter and also the switching voltage is half of the output voltage is value occurred

DOI : http://dx.doi.org/10.20902/IJCTR.2018.110404

(Yang, Liang, & Chen, 2009). In this paper, a converter with high static gain with reduced switching stress is proposed based on the SEPIC converter design. Compared with other converters, the proposed method gives reduced input inrush current for inductor whereas switching frequency is less in the proposed configuration.,

This paper is organized as follows: Section 2describes the DC-DC converters operation and compares the boost and SEPIC with its merits and demerits. Section 3presents the design of the proposed converter and its operation along with the chosen parameters. In Section 4the analysis and results for the various DC-DC converters along with the proposed converter are explained briefly.The paper concludes the performance merits of the proposed converter in Section 5.

2. DC-DC converter

The converter is used to convert variable dc voltage to the fixed dc voltage for many DC applications/ The boost converter is a conventional high step up converter used in high voltage applications. The boost converter is based on the step-up principle used for output voltage which is greater than the input voltage and its circuit model [6],as shown in Fig. 1.

To enhance the efficiency of the boost converter, it is linked with both coupled inductor and switched capacitor. During the period of high step up operation, current ripple is higher in the power devices and brings out conduction loss which turns off the current,. The boost converter is upgraded as the conventional interleaved boost converter, in order to improve the efficiency. [9]. To reduce the current ripple by using two switches but it creates reverse recovery problem in the diode.

The single-ended primary inductor converter (SEPIC) operates based on the principle of both step-up and step-down converters. It contains of two inductors for buck or boost action of the input voltage gives non inverted output, as shown in Fig. 2. It this converter the energy will be transferred through capacitor C_1 and inductor L_1; for the reason that, the switching voltage is greater than the boost converter. The static gain of the converter applied for numerous input voltage application. The voltage across the switch is nearly equal to the addition of both input and output voltages. The inrush input current for inductor L1 is minimized when equated to the boost converter but it has voltage stress.

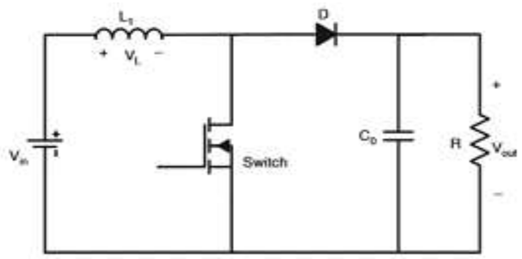

Fig. 1. Boost converter circuit

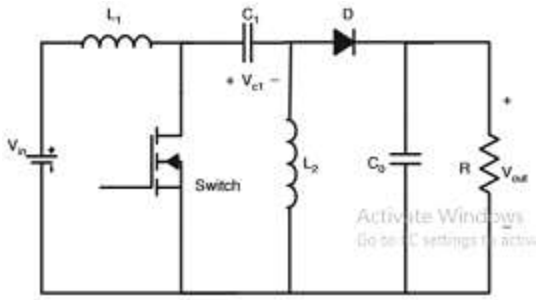

Fig. 2.SEPIC converter circuit.

Modification of the conventional SEPIC converter by adding diode D_M and capacitor C_2 [6], in the converter circuit as in Fig. 3. It is the amalgamation of the SEPIC and boost converter which enhances the static gain. By using the conventional boost converter's output voltage, capacitor the C_1 and C2 gets charged, because of the static gain.

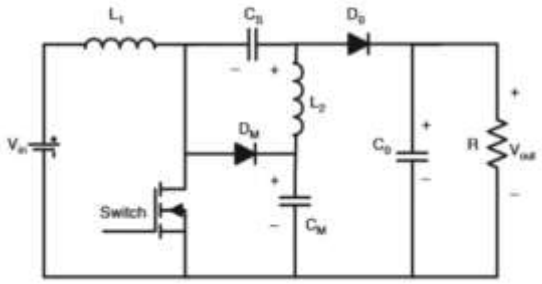

Fig. 3. Modified SEPIC converter circuit

The static gain is increased by two and the switching voltage is minimized to half of the value compared to the boost converter. Large input inductor is needed in order to reduce high startup inrush current which flows through the inductor L_1, and to reduce that. It involves soft switching techniques for turn ON and turn OFF condition for all small input voltages.

3. Proposed converter

The proposed converter is shown in Fig. 4, with modification on the SEPIC converter to advance the system performance and the inductor L1 inrush current is minimized. The proposed topology also works in the principle of both boost and SEPIC mode but the output capacitor connection is slightly modified in this configuration. The proposed converter minimizes the inrush current for inductor L_1 and advance the operation of the converter compared to other converters.

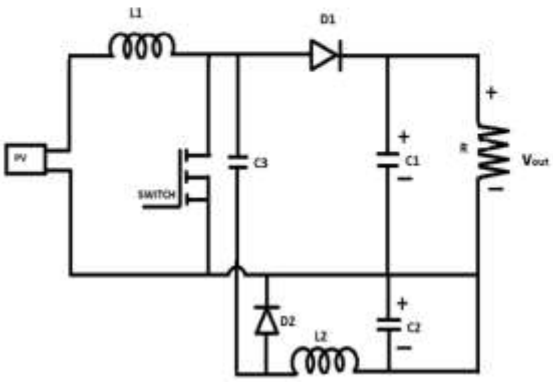

Fig. 4.Proposed converter circuit.

It also minimizes the stress and the low voltage for switching is utilized in the converter for high voltage conversion. It consists of one switch S, two diodes D_0 and D_M, and three capacitors C_1, C_2 and C_S, and two inductors L_1 and L_2. The converter output voltage is almost equal to the sum of C1 and C2 capacitors voltage.

3.1 Principle of operation and analysis

The proposed hybrid topology (Fig 4) is examined based on the idea that the converter works in continuous conduction mode and all parameters are ideal. In accordance with, the following three operating modes is explained:

Modes of operation A [t_1–t_2] (Fig. 4(a)): In this mode the system operation is effective when the power switch S is *ON*. The inductors L_1 and L_2 are gets charging whereas capacitor C_3 is in discharging mode. At the same time both Diodes D_1 and D_2 are in blocked condition by the negative voltages V_{C1} and$V_{C3.}$

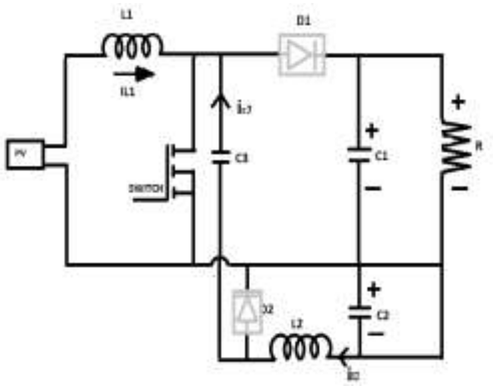

Fig. 4(a). Mode A

Mode of operation B [t_2–t_3] (Fig.4(b)): When the power switch S is turned *OFF* this operating mode happens when the voltage across the capacitor C_1 is greater than the voltage across the capacitor C_3. During this operation capacitor C_3 gets charged (the voltage across this capacitor will increase) and the inductors L_1 and L_2 energy is discharging. Diode D1 gets blocked but Diode D2 is in ON state.

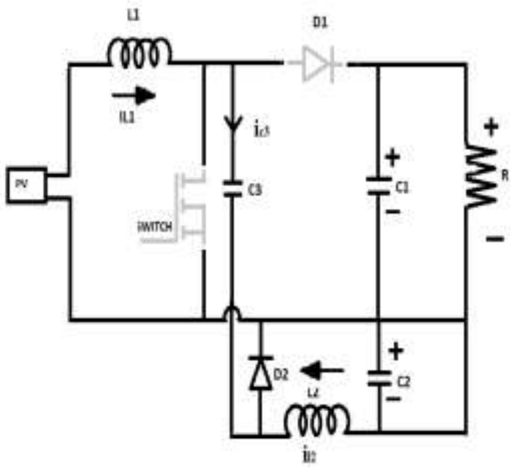

Fig. 4(b). Mode B

Modes of operation C [t_3–t_4] (Fig. 4(b)): This operating mode appears when the power switch S is turned *OFF* and voltage across capacitor C_3 is greater than or equal to the voltage across capacitor C_1. Both inductors are in discharging state and the inductor current L_1starts flow capacitors C_1 and C_3 gets charged. Both diodes are in *ON state*.

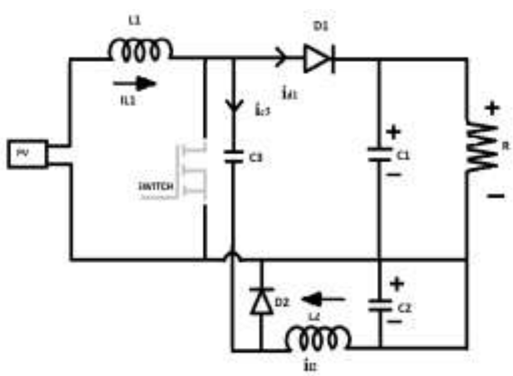

Fig. 4(c). Mode C

Table I. Parameter for Proposed Converter

Parameters	Existing system	Proposed system
Switching frequency	4khz	2khz
Duty cycle	70%	70%
Inrush current	5amps	3.1amps

The capacitor C_2 voltage is equal to the voltage across all diodes and power switch. The output voltage is nearly equal to the addition of the capacitor voltage C_1 and C_2.The equation was obtained for the proposed converter to estimate the inductance and capacitance using the conventional method.

The proposed converter static gain relied on the average inductance voltage with zero steady state. The duty cycle relation is obtained in Eq.(1) considering continuous conduction mode operation. The relationship of Duty cycle for the proposed converter is a integration of both boost and SEPIC converters. The output voltage of the converter is more than that of the conventional boost and SEPIC converter.

The prolonged static voltage gain of the proposed hybrid DC-DCconverter in Continua's Conduction Mode is the sum of the two voltage ratios (or gains) of the conventional converters Shown in fig 4 ,given in Eq.(1),

$$\frac{V_0}{V_1} = \frac{1+\delta}{1-\delta} \quad (1)$$

The inductorL_1 can be defined by following Eq. (2), where $v_i$is the maximum PV output voltage at Maximum Power Point

$$L_1 = \frac{V_i \delta T}{\Delta i_{L_1}} (2)$$

The computation of the inductor L_2 can be achieved by applying the same method. Accordingly, the inductor L_2 can be expressed by Eq.(3).

$$L_2 = \frac{V_{C_2}(1-\delta)T}{\Delta i_{L_2}} (3)$$

For the capacitors C_1 and C_3 a same procedure can be used, taking into the account of a limited voltage ripple comparatively to the average voltage value of every single capacitor. The capacitors discharging times consider as Dt_1 and Dt_2 as a function of the duty-cycle d, likewise in the inductors. but it only suitable in steady state operation. Consequently, in order to ensure a accurate dynamic behavior, The discharging times Dt_1 and Dt_2 is considered as the settling times of the currents in inductors andL_2 and $P_o$refers *to* the load power, giving Eq.(4),

$$C_3 = \frac{1}{\Delta V_{C_3}} \frac{P_0}{V_0} \Delta t_2 (4)$$

The rate of the capacitor C_2 can be acquired and considering that charge the modification of the capacitor DQ is related with the current modification in inductor L_2 D i_{L2}. The C_2 capacitor can be obtained from Eq. (5).

$$C_2 = \frac{T \Delta i_{L_2}}{8\, \Delta V_{C_2}} (5)$$

4. Results and discussion

The proposed topology is shown in Fig. 4havebeen simulated using MATLAB/Simulink to validate the above design considerations as well as to check their system performance and operations. The proposed converter output voltage simulation diagram is shown in Fig. 5.From Fig. 8,itis noted that the proposed converter (150 V) output voltage is attained and static gain is enhanced. The PV system is to afford toomany power is possible by the solar radiation. In order to achieve the maximum power, MPPT (Maximum Power Point Tracking) should be incorporated in the system. This technique tracks the maximum power point irrespective of the environmental condition.

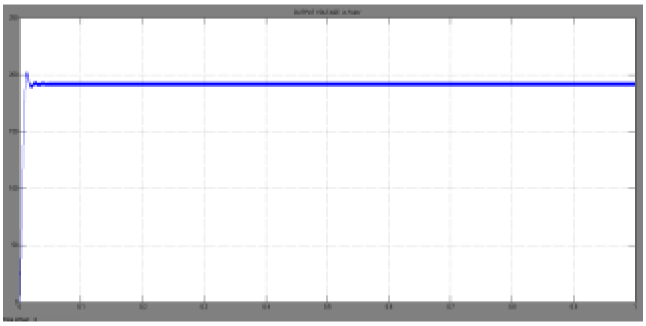

Fig. 5. Simulation result of the output voltage

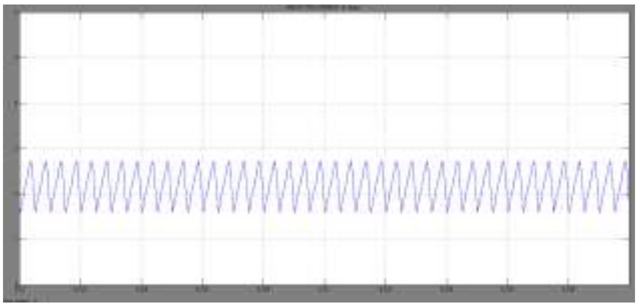

Fig. 6. Simulation result of the output current inductor (i_{L1})

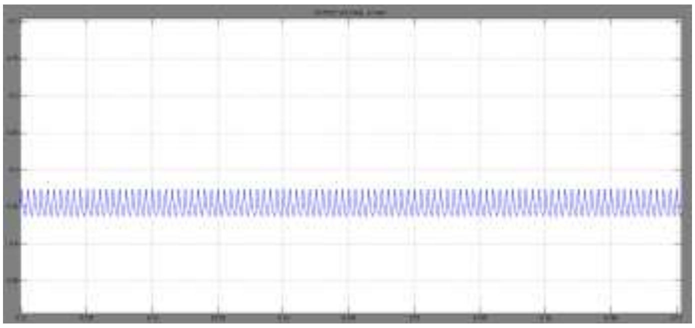

Fig. 7. Simulation result of the output current inductor (i_{L2})

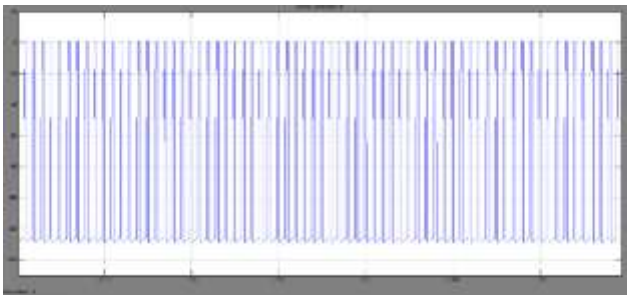

Fig. 8. Simulation result of the voltage across the diode (D1)

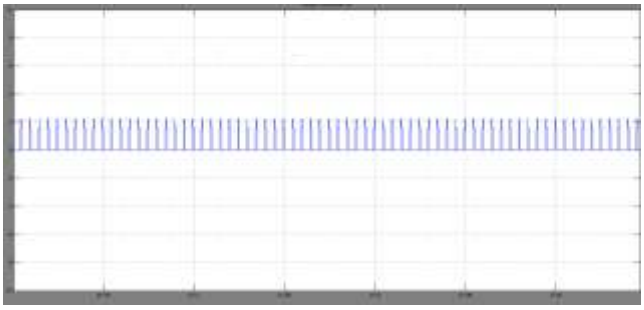

Fig. 9. Simulation result of the current through the diode (D1)

5. Conclusions

In this paper a novel high-gain single-switch non-isolated DC-DC converter is recommended. . An MPPTalgorithm was applied in order to control the voltage of the proposed converter. This system is characterized by the combination of a Boost and SEPIC DC-DCconverters, by means of only one controlled power switch, and is opted for photovoltaic applications, where low voltage solar panels are incorporated with MPPT, used to provide high DC voltage. The proposed topology practices two loading capacitors with equal rating rather than one capacitor in the SEPIC model. These capacitors divide up the voltage stress and the inrush current. The switching frequency is reduced compared to proposed converter. The proposed topology facilitates an extended voltage static gain, when related with the conventional boost and SEPIC converters, while reducing the voltage stress across the power switch and diodes, being lesser than the output voltage of the converter. Simulation and experimental results were shown in order to validate the characteristics of the proposed system as well as its potential to trace the maximum power point of a photovoltaic panel and that it can be well chosen for various renewable applications with simple model and high efficacy.

References

1. Al-Saffar, M. A., & Ismail, E. H. , “A high voltage ratio and low stress DC–DC converter with reduced input current ripple for fuel cell source,” Renewable Energy, Vol. 82, october 2015, pp. 35–43.
2. Chiang, S. J., Shieh, H. J., & Ch`en, M. C., “Modeling and control ofPV charger system with SEPIC converter*,”* IEEE Transactionson Industrial Electronics, vol*.* *56*, No. 11, November 2009, pp. 4344–4353.
3. Fathabadi, H.,“Novel high efficiency DC/DC boost converter for using inphotovoltaic systems,” Sol Energy vol. 125, February 2016, pp. 22–31
4. Fardoun, A. A., & Ismail, E. H., “Ultra step-up DC–DC converter with reduced switch stress,” IEEE Transactions on Industry Applications, vol. *46*, No. 5, October 2010, pp. 2025–2034.
5. Figueres, E., Garcerá, G., Sandia, J., Gonzalez-Espin, F., & Rubio, J. C. , “Sensitivity study of the dynamics of three-phase photovoltaic inverters with an LCL grid filter,” IEEET ransactions on Industrial Electronics, vol. *56*, No. 3, March2009, pp. 706–717.
6. Gules, R., Dos Santos, W. M., Dos Reis, F. A., Romaneli, E. F. R., & Badin, A. A., “A modified SEPIC converter with high static gain for renewable applications,” IEEE Transactions onPower Electronics, vol. *29*, No. 11, November 2014, pp. 5860–5871.
7. Hart, D. W. Power Electronics. India, Pakistan, Nepal, Bangladesh, SriLanka, Bhutan: Tata McGraw-Hill 2011.
8. Hsieh, Y. P., Chen, J. F., Liang, T. J., & Yang, L. S., “Novel high step-upDC–DC converter for distributed generation system,” IEEE TransactionsonIndustrial Electronics, vol.60, No. 4, April 2013, pp.1473–1482.
9. Huang, X., Wang, X., Nergaard, T., Lai, J. S., Xu, X., & Zhu, L., “Parasiticringing and design issues of digitally controlled high power interleaved boost converters,” IEEE Transactions on Power Electronics, vol. 19, No. 5, September 2004, pp. 1341–1352.
10. Jacobson, M.Z., Delucchi, M.A., “Providing all global energy with wind, water, and solar power, part I: technologies, energy resources, quantities and areas of infrastructure, and materials” Energy Policy vol. 39, No. 3, March 2011, pp.1154–1169.

11. Kesraoui, M., Korichi, N., & Belkadi, A. “Maximum power point tracker of wind energy conversion system,” Renewable Energy, vol. *36*, No 10, May 2010, pp. 2655–2662.
12. Kim, J. K., & Moon, G. W. “Derivation, analysis, and comparison of non-isolated single switch high step-up converters with low voltage stress,” IEEE Transactions on Power Electronics, vol. *30*, No. 3, March 2015 pp. 1336–1344.

*****