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Performance Measures of an Efficient Compensator Design for a Buck Converter

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Abstract : Traditional Ziegler–Nichols method is well known adapted control scheme for feedback control system. However it provides limited control performance with increased controller gain. It is proposed here an efficient compensator based on bode plot and root locus method to improve control performance for a buck converter. This is tested with three different control objectives.
Keywords : PI, PID, Ziegler–Nichols Z-N,Rise time, Settling time, Band width.

1. Introduction

Switched-mode dc–dc converters are very popular because of their high efficiency and compact size which convert one level of electrical voltage into another level by switching action [1-2]. They have been widely used in medical electronics, adapters of consumer electronics products, communication industry, personal computers and computer peripherals [1-5].These converters inherently shows time-variant, nonlinear dynamic characteristics due to switching, power devices, and passive components, such as inductors, and capacitors. Linear control techniques need a dynamic model of the switching converter to design the feedback compensation. As a result, the conventional linear control techniques cannot be directly applied to analyse the dc-dc converter. Dynamic modelling allows the low frequency behaviour of the system, and leaves the insignificant high switching frequency. It needs low frequency approximation of converters to neglect the high frequency phenomena. The inherent switching operation of power electronic converters results in the circuit components being connected together in periodic changing configurations. They represent different circuit configurations within each switching cycle.Thesudden load changes introduced by modern processorsmake the dynamic response of a conventional power-supply system too slow to track the changes, so dynamic response of power supplies is so significant in this respect[2].Ziegler–Nichols step response method is a classical approach for PID controller feedback control systems has good disturbance rejection. But the controlled response would have high-percent peak overshoot, and the control signal requirement is also high, which-in turn lead the actuator to saturation[4].

Peretz et.al has developed a time-domain based digital controller of pulse width modulation for dc–dc converters. A digital PID template is used to fit the desired response. The proposed work carried out in the time

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domain which bypasses errors related to the transformation from the continuous to discrete domain and to discretization[3].A dc-dc boost converter that has a practical inductor and a series resistance which exhibits highly nonlinear and non-minimum phase properties; it is not an easy task to design a controller that is robust against load perturbations. The steady-state performance of a dc-dc converter can degrade due to inherent time delay in ADC while implementing digital controller. Reference [5] have made three modifications to the digital PID controllers to improve their steady-state performance such as dead zone, an averaging digital filter and two sets of gains.Tan et.al [6] has proposed family of fixed-frequency pulse width-modulation-based sliding-mode voltage controllers operating in the discontinuous conduction mode for buck, boost and buck–boost converters.

Synergetic theory to the control of a boost converter is introduced in [7] have two different implementations of a control law that limits inductor current overshoot dynamic adaptation of the control parameter depending on the output voltage error. It gives a better trade-off between transient and steady-state performance. Second control law that uses an integral error term to eliminate steady-state error i.e. control law that uses the high-pass-filtered inductor current and does not require knowledge of the reference current, which is load dependent for a desired output voltage. A complementary proportional-integral-differential (PID) controller to the PD-PBC has been designed for removing the steady state error owing to the parasitic resistance [8].Digitally controlled dc-dc converter the output voltageregulationis circumscribed of the within comparative narrow ranges ofthe input voltage and the load, and that increasing the integral gain of the digital control circuit to extendthe regulation range, will lead to deterioration in the dynamic characteristics ofthe converter [10].Derivative term of conventional PID controller injects noise in the feedback loop due to the series resistance and equivalent series inductance (ESR, ESL) of the output capacitor.

These parasitic parameters may cause the large overshoot or undershoot during large signal transient.

Discrete jumps at switching transitions with alternating polarities occur during a small-signal transient or even at the steady state due to the ESR [3-4]. Due to the discrete jump cause degraded phase margin even though derivative gain is added to improve the phase margin, the increase in gain may be insufficient. Although the phase margin can be improved by reducing the cut off frequency of the low-pass filter associated with a practical differentiator circuit, closed-loop bandwidth is compromised [11].Conventional PID controllers use single loop voltage control as feedback loop which is not suitable for changing supply and load conditions.

The power converter requires very tight output voltage regulation which enforces challenge of very good controller to meet the parameter variations. The parameter variations such as large supply and load variations, non-linearity in the converter operation makes traditional PID controllers are not suitable. Controller needs to operate at an infinite switching frequency in order to track the reference signal to achieve the better performance both dynamic as well as steady state operation. This may cause high switching losses, core losses in inductor and transformer, and electromagnetic interference (EMI) problems. The commercially viable analog controllers use P or PI control with voltage feedback in control loop.

The proposed work replaces the problems of classical PID tuning by Z-N methods by an efficient compensator designwhich is based on the phase margin criteria and location of roots usingbode plotand root locustechnique respectively. To place the poles in any arbitrary location feedback should be applied on all the state variables.Section 2.is presents the problem formulation for a buck converter. Results and discussion is given in section 3 followed by conclusion in section 4.The compensator design for this work is not elaborately discussed in this paper since they will be reserved for the later publication by the author.

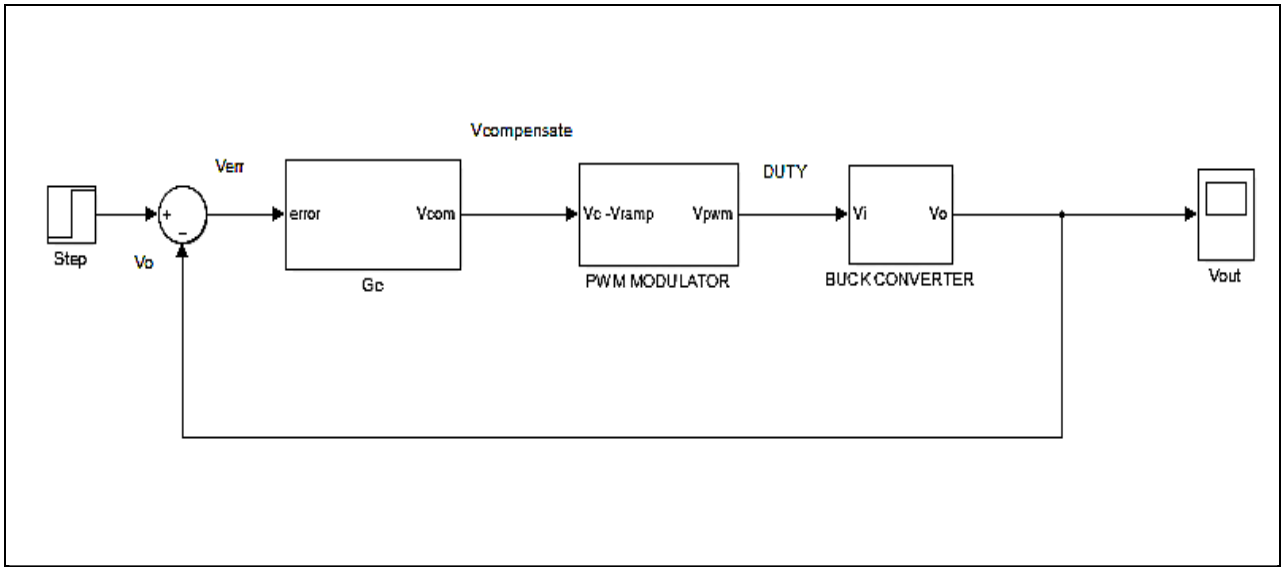

Figure1The proposed converter scheme

2. Problem formulation

Figure1 gives the proposed buck converter with controller scheme. The buck converter transfer function [9] for output to duty ratio is given in equation 1.

$$\frac{V_O}{\delta(s)} = V_I \frac{R_{ESR}Cs+1}{LCs^2+\left(\frac{L}{R_O}+C(R+R_{ESR})\right)s+1} \quad (1)$$

Where, R_{ESR} is the equivalent series resistance of the output capacitor, L is inductance of the converter, and C output capacitance.

The location of twin poles are given by

$$f_p = \frac{1}{2\pi\sqrt{LC}} \quad \text{and} \quad \text{zeros at} \quad f_Z = \frac{1}{2\pi R_{ESR}C} \quad (2)$$

The transfer function for PWM stage [9]is given by

$$\frac{V_O(s)}{V_C(s)} = \frac{1}{V_M} \quad (3)$$

Where, VM is ramp in magnitude in the PWM stage and DC gain for this stage is nothing but ratio of input voltage VI to VM.

From equation (1) and equation (3), the open loop transfer function for the output Vo with respect to the compensation network control voltage Vc is:

$$\frac{V_O}{V_C(s)} = \frac{V_I}{V_{M\ I}} \frac{R_{ESR}Cs+1}{LCs^2+\left(\frac{L}{R_O}+C(R+R_{ESR})\right)s+1} \quad (4)$$

The power stage of the buck converter [3] is given below

$$G_P(s) = \frac{3.333*10^8}{s^2 + 2500s + 1.333*10^8} \quad (5)$$

The aim of the controller is to find the duty cycle δ as function of states of the output voltage V_o, input voltage V_I, and the inductor current I_{LI}.The control algorithm forces the state error reach zero following the control signal.

3. Results and Discussion

The simulation diagram is shown in figure 2.The compensator diagram and modulatorare omitted in order to give simple and clear depiction of circuit diagram. The input voltage for the converter is 120 V and the output voltage is 60 V.

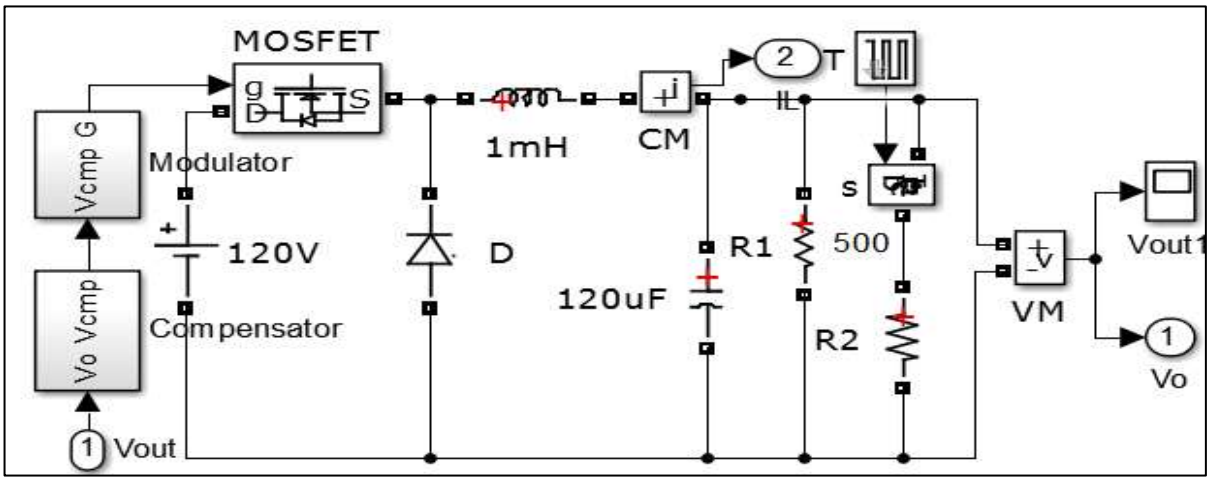

Figure 2 Simulation diagram Buck Converter

The table1 provides the results for PIDtuned values three different control objectives.

Table1 PID values for different cases Buck Converter

Sample	K_P	K_I	K_D
Case 1	2.4248	1301.2432	0.0002
Case 2	5.7314	6345.36	0.0005
Case 3	48.6369	212410.1038	0.0021

Table 2 Performance measures for different cases Buck Converter

Sample	Rise time (sec)	Settling time (sec)	PeakOver-shoot (%)
Case 1	1.94e-5	0.00424	16.9
Case 2	9.03e-6	0.0012	14.3
Case 3	2.06e-6	1.65e-5	4.31

Performance measures such as rise time settling time and peak overshoots for three different cases buck converter is given in table 2.

Table 3 Phase margin stability analysis for different cases of Buck Converter

Sample	Phase margin	Stability
Case1	52	Stable
Case2	56	Stable
Case3	68	Stable

The phase margin and stability analysis of bode plots are given in table3.The peak overshoot which is below 5 percentage in the 3rd case which gives very smaller values rise time and settling time.

The figures 3a, 4a and 5a provide the open loop transfer function of the converter. Figures 3b, 4b and 5b give corresponding closed loop response for the values given in table1 – table3.

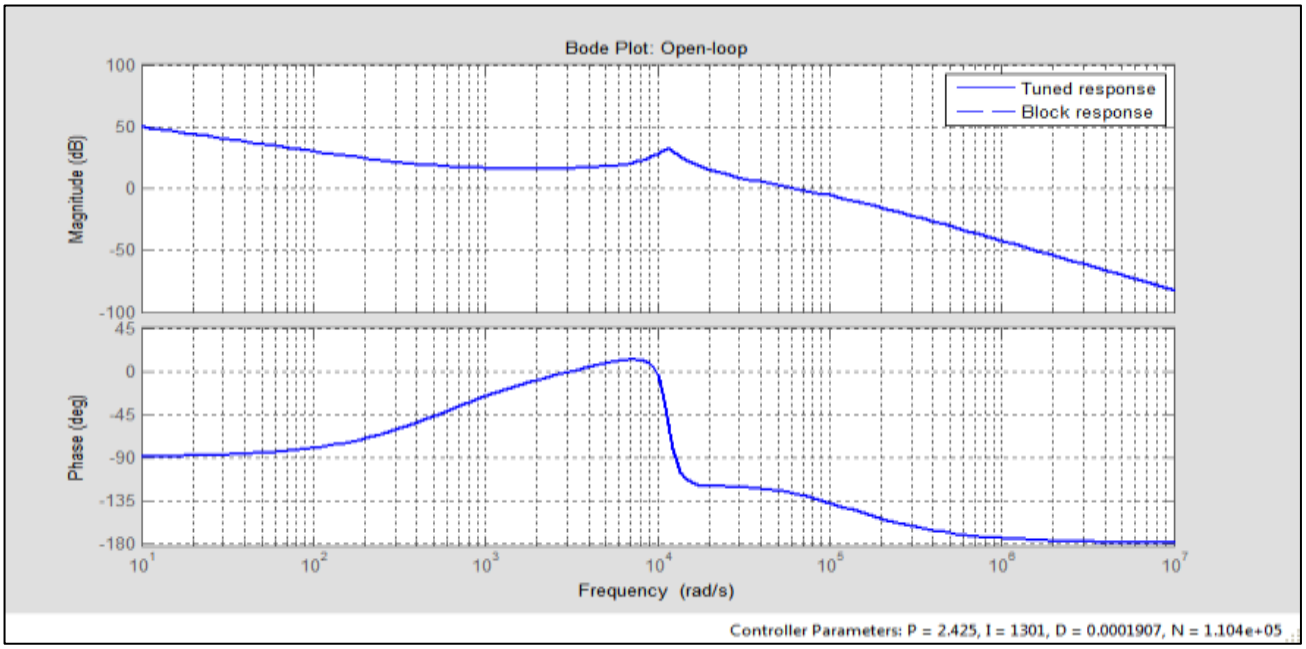

Figure 3a Bode plot for open loop Buck Converter

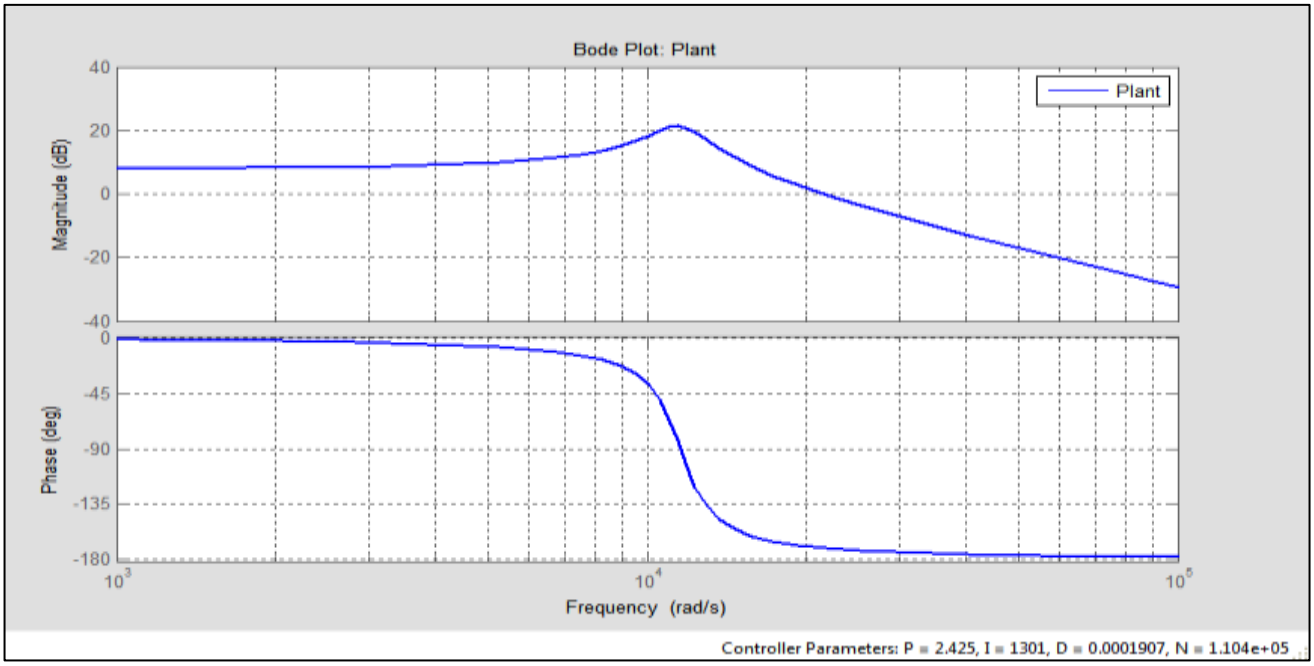

Figure 3b Bode plot closed loop of Buck Converter

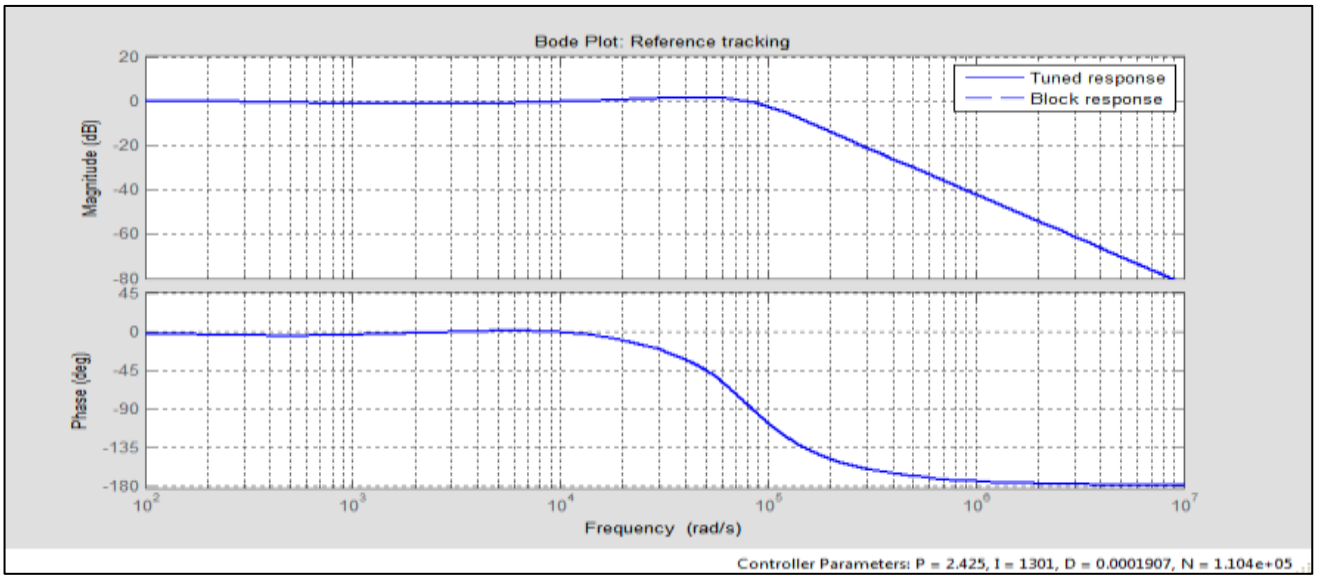

Figure 3c Bode plot reference tracking of Buck Converter

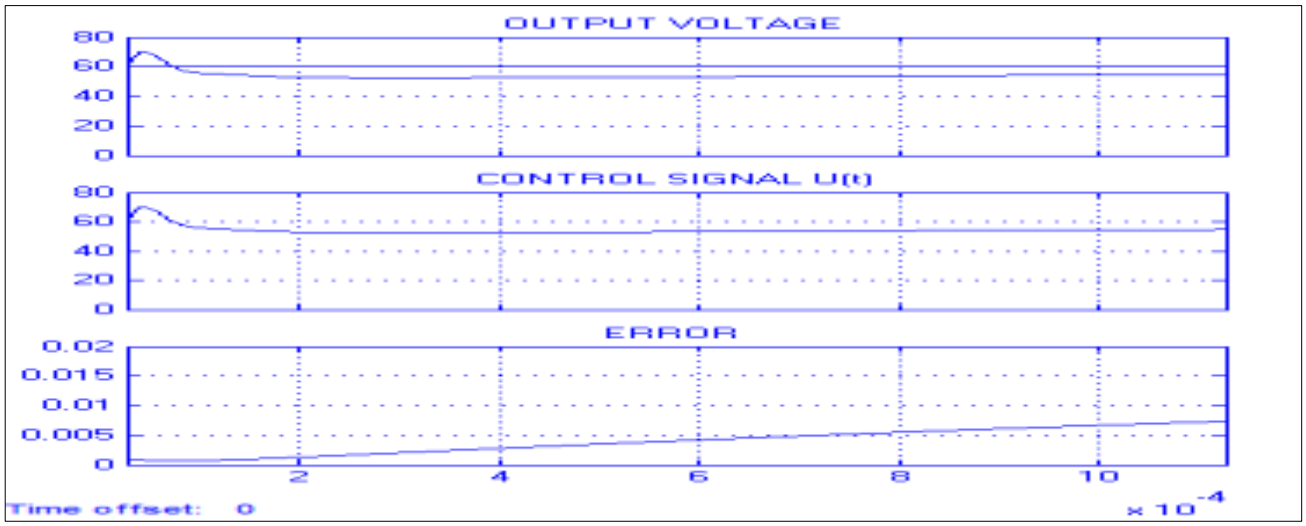

Figure 3d Simulation results for Case 1 Buck Converter

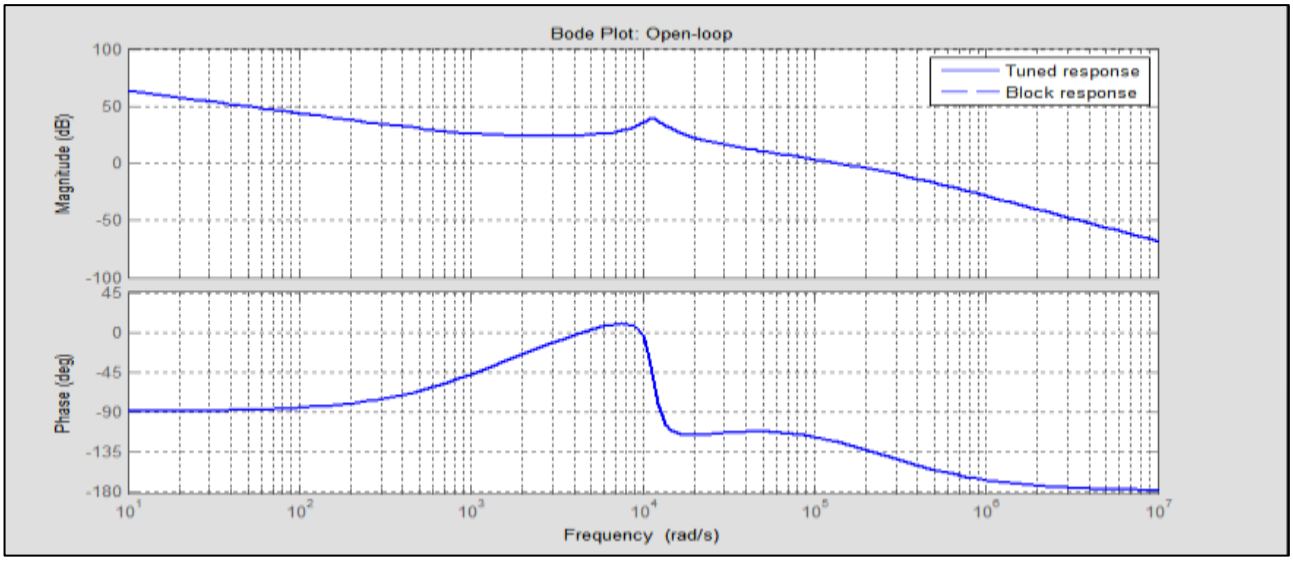

Figure 4a Bode plot for open loop Buck Converter

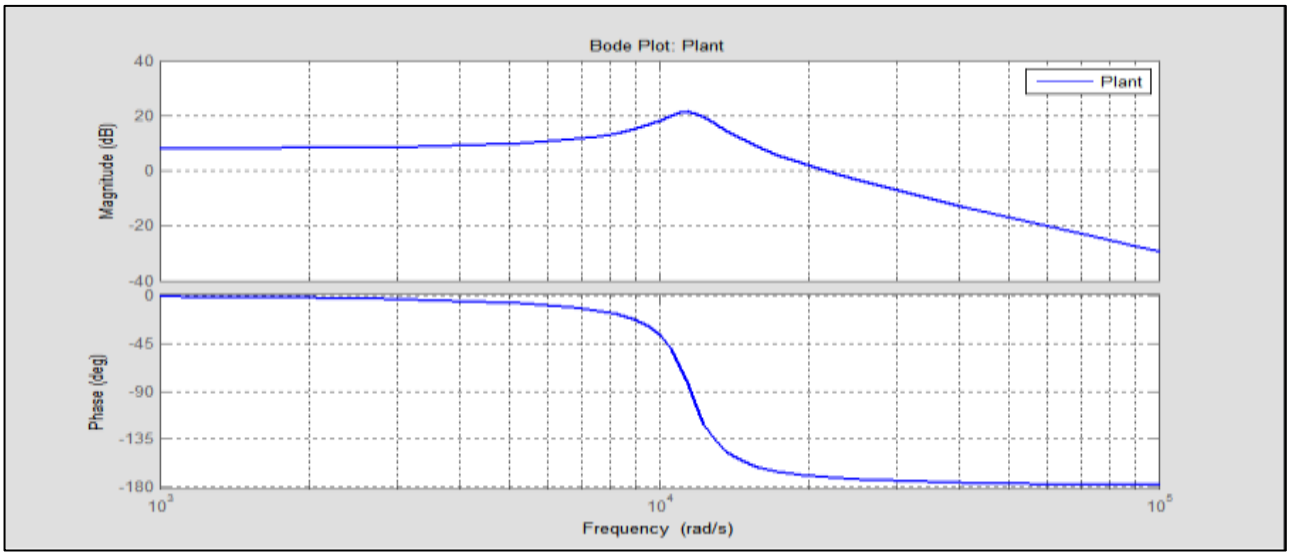

Figure 4b Bode plot closed loop of Buck Converter

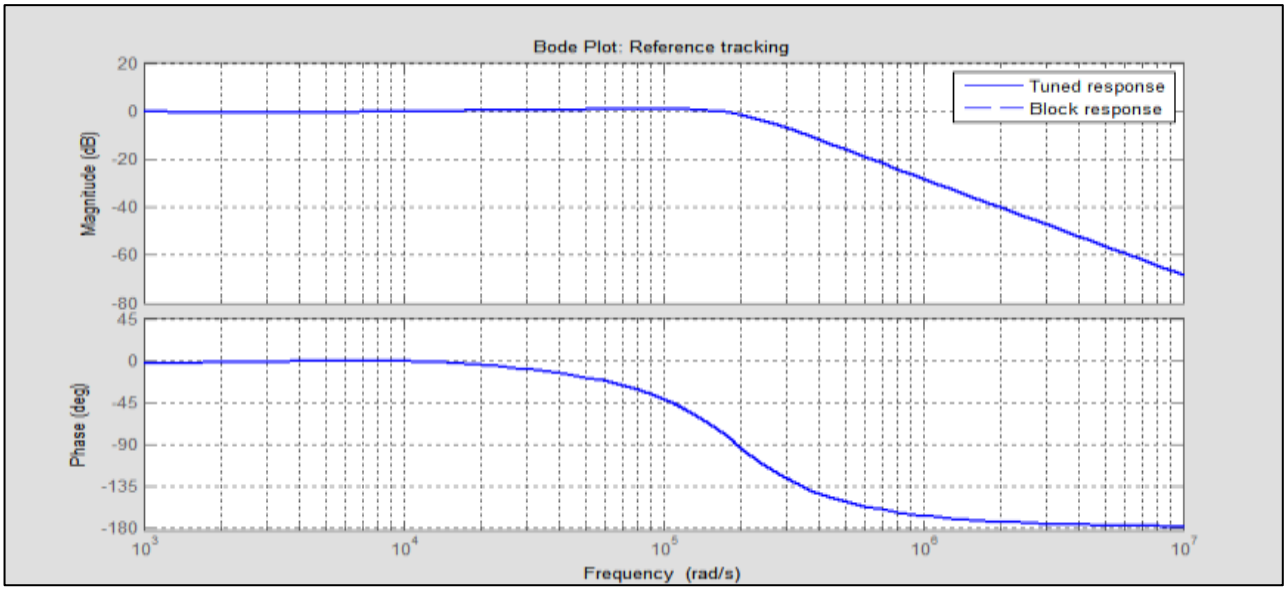

Figure 4c Bode plot reference tracking of Buck Converter

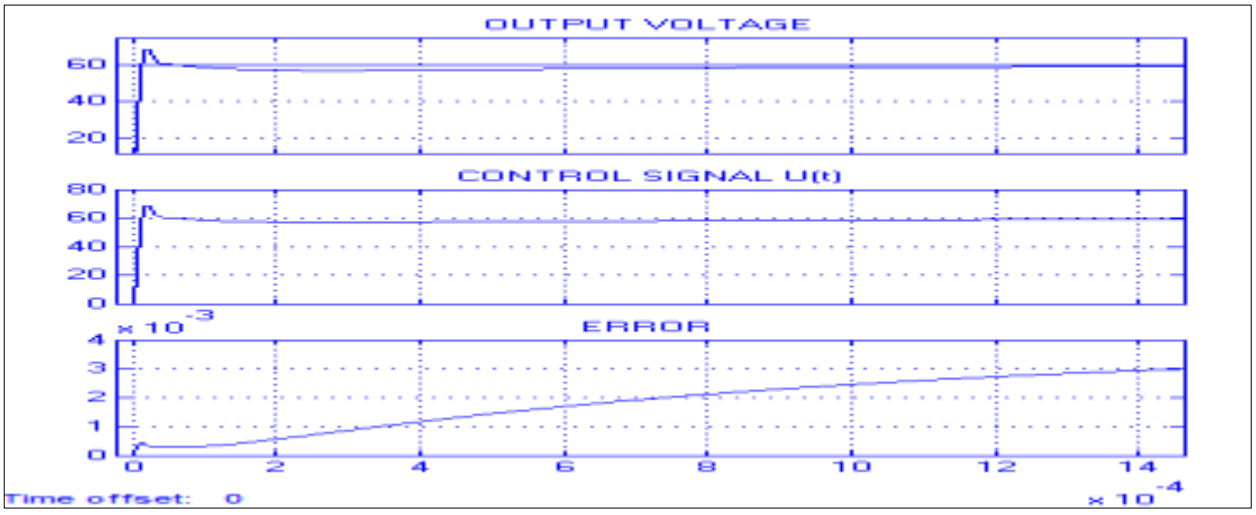

Figure 4d Simulation results for Case 1 Buck Converter

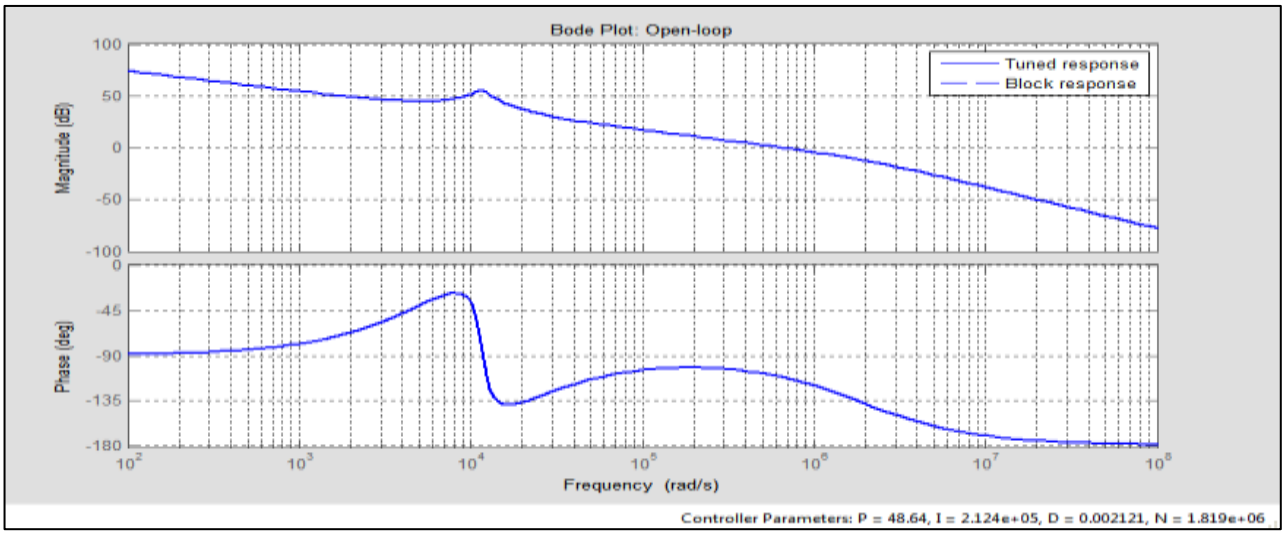

Figure 5a Bode plot for open loop Buck Converter

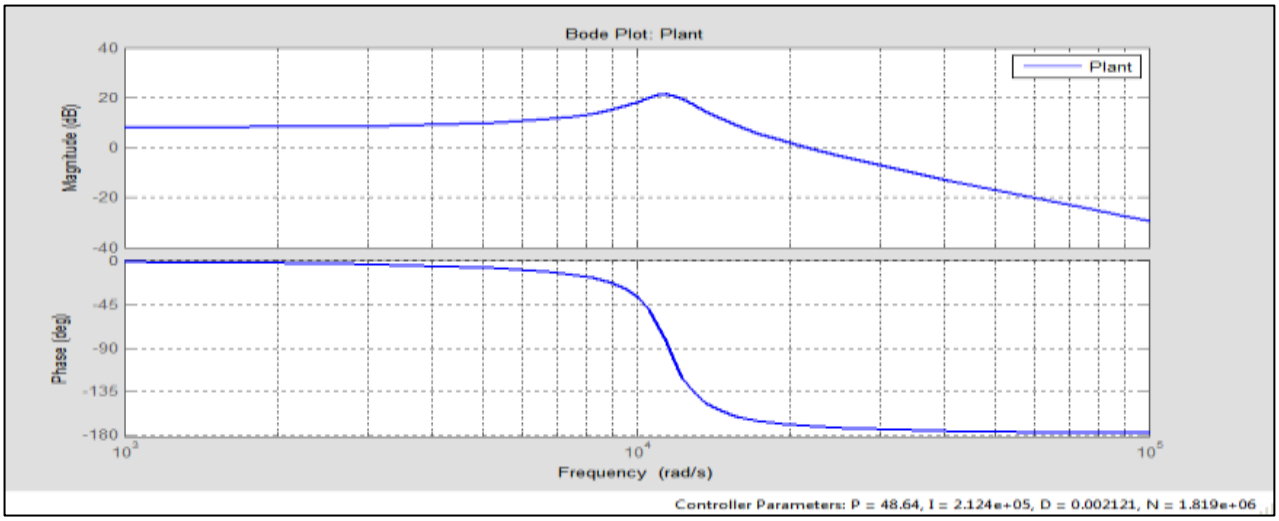

Figure 5b Bode plot closed loop of Buck Converter

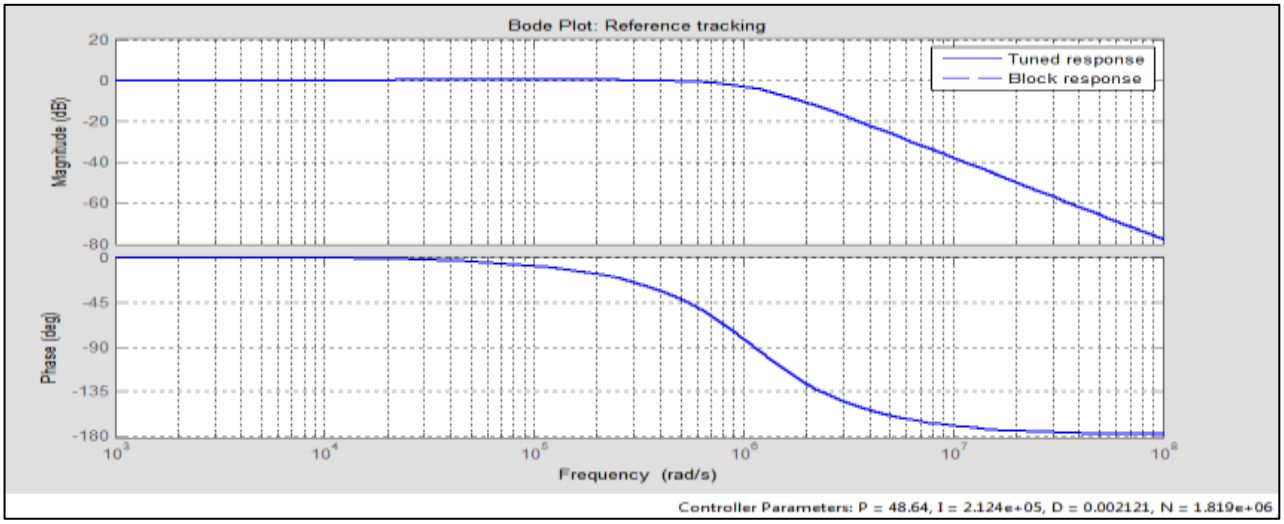

Figure 5c Bode plot for reference tracking of Buck Converter

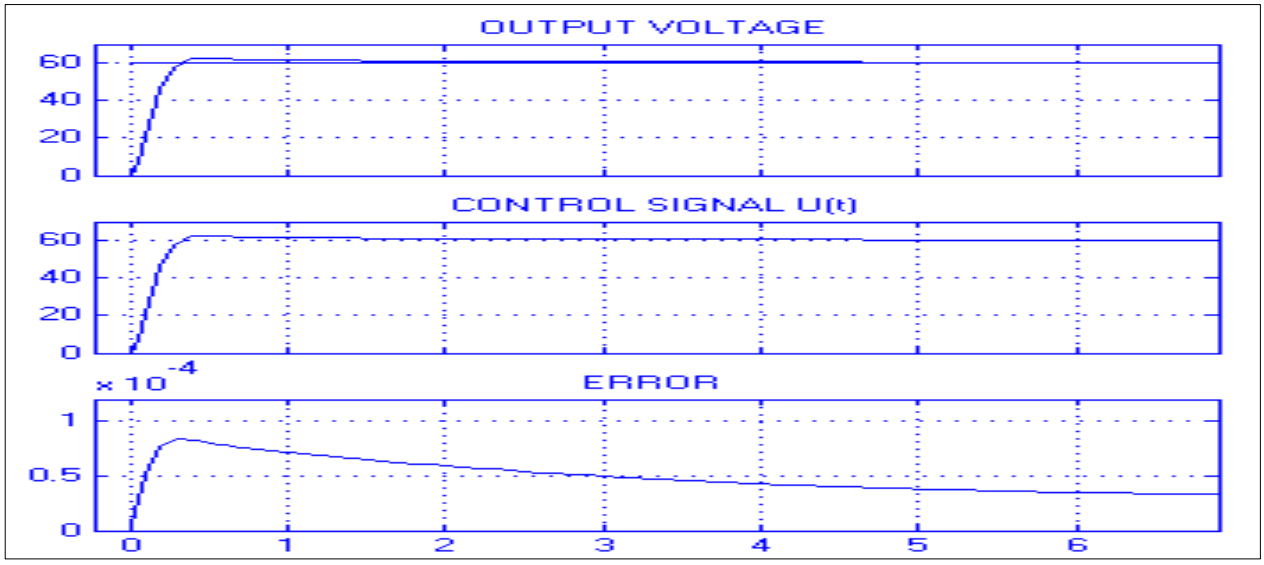

Figure 5d Simulation results for Case3 Buck Converter

Figure 3d -5d shows the simulation results for case1-case3. From the simulation results it is obvious that sample case3 provides better performance compared to case1-case2.The performance measures such as peak over shoot, rise time, settling time are improved. The peak overshoot for case3 is below 5% with reduced rise time and settling time.

4. Conclusion

Conventional tuning of PID control by Ziegler–Nicholsmethod gives very limited control performance. This problem is overcome by an efficient compensator design based on bode plot and root locus technique proposed here which outperforms in terms performance measures such as peak overshoot, rise time, settling time. The proposed control algorithm is tested three different cases which also guarantee the stable operation in addition to good control performances.

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