

# **International Journal of ChemTech Research**

CODEN (USA): IJCRGG, ISSN: 0974-4290, ISSN(Online):2455-9555 Vol.11 No.04, pp 01-15, **2018** 

ChemTech

# Half Bridge Bidirectional Resonant Dc-Dc Converter

C.Rajeswari<sup>1</sup>\*,M.Santhi<sup>2</sup>

# Solaimali College of Engg & Tech, Veerapanjan, Madurai, Tamilnadu, India Sethu Institute of Techonolgy, Kariapatti, Tamilnadu, 625 020 India,

**Abstract :** Current applications hope for the model of dc-dc convertor to be proficient with more power intensity and low Electromagnetic interference (EMI). Frequent functioning of switches to attain more power density leads to switching losses. Practical use of a phase-shift full bridge exhibits some major flaws. Those are power losses due to circulating current, voltage fluctuation across rectifier diodes and ZVS choice of switches. Additional circuitry, essential to eradicate these issues, needs complex design. Thus, the association of a resonant and Dual Active Bridge Converter (DAB) forms bidirectional dc-dc converter to compensate moderate voltage request. In case of normal load the converter shots at resonance. Primary side has zero voltage turn on (ZVS) and achieves zero current turn off (ZCS) at secondary. In case of overload, the resonant capacitor voltage is compressed by parallel diode and the converter maintains dual mode of resonant and DAB. The proposed converter is conveyed in terms of strategy scheme of all devices, time domain wave form, dual power usage, efficiency and state trajectory.

Keywords : Dual Active Bridge Converter(DAB), ZCS, ZVS, electromagnetic interference.

# 1. Introduction

A phase-shift full bridge (PSFB) converter drives with low phase-shift value for standard inputs. For extensive input, PSFB increases the range leading to over current with conduction losses. Inclusion of circuits makes the converter more complex and affects control strategy. An alternative is PSFB series resonant converter. The converter appraises the turn ratio of the transformer. Even though, it overcomes the above said issues, it fails to operate on wide input range. The net result is high peak current with lowered efficiency.

Surge energy is stored in the leakage inductance of a transformer. Preceding studies imports voltage doubler, multiplier rectifier and an active-clamp circuit to absorb surge energy. The circuit's step-up ability is exploited as boost converter. The circuit avoids snubber at the output stage. In our work, we propose a novel hybrid-type PSFB series-resonant converter integrated with an active-clamp step-up converter with voltage doubler. This integration of various control plans operate in two modes. When voltage lags behind the standard, the converteris adapted as an active-clamp step-up converter. Step-up function is achieved by exploiting active-clamp circuit on primary side and voltage doubler rectifier across the output. The converter is retained as a PSFB series-resonant converter for regular values. High efficiency is accomplished by implying lenient

# International Journal of ChemTech Research, 2018,11(04): 01-15

DOI : http://dx.doi.org/10.20902/IJCTR.2018.110401

switching techniques on primary switches and rectifier diodes. Thus the hybrid operation enables the proposed converter to provide larger phase-shift value with reduced conduction losses. Thus it leads the conventional type.

# 2. Related Works

Dual active bridge (DAB) converter is introduced to exclude the concerns related to dc-dc conversion. The proposed is a grouping of reliable DAB and LLC resonant converter. The resonant tank comprises of the resonant capacitors in the lower voltage region. The capacitors are clamped to the output voltage via clamping diodes. This paper presents an improved V-I characteristic curve of LLC in the presence of DAB approach. Observation of V-I curve enables the control of measured output voltage. Thus regulation of duty cycle and output current limit can be noted. Thus the switching frequency is fixed to avoid switching loss. The simple structure examines every cycle for its current limitation.

## 3. Proposed Methodology

#### **3.1 Introduction:**

The association of a resonant and dual active bridge converter (DAB) forms bidirectional dc-dc converter to compensate moderate voltage request. In case of normal load the converter shots at resonance. Primary side has zero voltage turn on (ZVS) and achieves zero current turn off (ZCS) at secondary. In case of overload, the resonant capacitor voltage is compressed by parallel diode and the converter maintains dual mode of resonant and DAB. The proposed converter is conveyed in terms of strategy scheme of all devices, time domain wave form, dual power usage, efficiency and state trajectory. Dual active bridge (DAB) converter is introduced to exclude the concerns related to dc-dc conversion. The proposed is a grouping of reliable DAB and LLC resonant converter. The resonant tank comprises of the resonant capacitors in the lower voltage region. The capacitors are clamped to the output voltage via clamping diodes. This paper presents an improved V-I characteristic curve of LLC in the presence of DAB approach. Observation of V-I curve enables the control of measured output voltage. Thus regulation of duty cycle and output current limit can be noted. Thus the switching frequency is fixed to avoid switching loss. The simple structure examines every cycle for its current limitation.



Figure 1Proposed DC-DC converter in SST application

## **Operation Principle**

The above circuit diagram is the proposed bidirectional dc-dc converter in SST application. The ac to dc conversion is realized on the high voltage side and dc to ac conversion through a LLC set-up on low voltage side. Bothfull bridge and half bridge switch network, for medium power SST application can be utilized at the hv side. The design features are

- a) Resonant circuit is located at the low voltage side.  $V_{LV_{dc}}$  remains constant.
- b) The resonant inductor Lscan be integrated with the transformer as the leakage inductance.
- c) The resonant capacitance is divided into Cr1shunted with D3 and Cr2 parallel with D4.

3

- d) Q1, Q2, Qr1 and Qr2 are switchesdesigned with bidirectional triggering. The capacitance of Cr1 resembles Cr2.
- e) Cdc1 and Cdc2 denote dc bus capacitors with large value of capacitance on high voltage (hv) side. It equally shares the total input voltage.Since the setup ideologies are similar, this work only aims on the analysis of power flow from hv side to lv side. Analysis is confined by nullifyingfreeloading capacitances of Q1, Q2, transformer, Qr1 and Qr2.

# 3.2.A. Normal Load Operation

The LLC dc-dc converter operates in open loop with the series resonant frequency  $f_s$  in (1) and reaches optimum efficiency.

 $f_{s} = \frac{1}{2\pi\sqrt{L_{s}(C_{r1} + C_{r2})}}(1)$ 

By means of graphical state-trajectory analysis [13-14], the steadystate trajectory of the proposed converter under normal load can be crafted as shown in Figure 2. Vcr1 taken along x-axis and ZriLs is taken along y-axis.

- Zr -impedance of the resonant tank
- iLs current through resonanant inductance

Vcr1 – voltage across Cr1.



Figure 2 Steady state trajectory of normal operation



Figure 3 Equivalent circuit of converter under normal operation



Figure 4 Steady state waveforms under OCP mode



Figure 5 Steady state trajectory of over current operation

$$Z_r = \sqrt{\frac{Ls}{Cr1 + Cr2}}(2)$$

The center point of  $V_{cr1}$  is  $V_{HV_dc}/2n$ . The radius depends on the load condition and increases with increase in load. zero radius means no load. Under normal operation, the radius is fixed as less than half of  $V_{LV_dc}$ , so that the voltage across  $C_{r1}$  will not be fastened from zero to  $V_{LV_dc}$ . D3 and D4 have Null current. Equivalent circuit of converter is shown in Figure 9. From the above Eqn, Itis inferred that when load exceeds  $2\pi Zr$ , D3 and D4 have Null current.

D4 will initiates default clamping voltage across Cr1 and Cr2.

$$r_{\text{nor}\leq}r_{\text{max}} = \frac{V_{h\nu\_dc}}{2n} = \frac{V_{l\nu\_dc}}{2}$$

$$\frac{g_{T_s}\frac{|iL_s|}{2}}{T_s} = I_{\text{Load}} \quad (3) \text{Where }, T_s = \frac{1}{f_s} \text{ and } R_{\text{crit}} = 2\pi Z_r(4)$$

#### **B.** Over Current Operation

The condition of over-current like short circuit rises the resonant current and hence the voltage across  $C_{r1}$  and  $C_{r2}$ . The order of shifting of state is from pure resonant mode to resonant and then to DAB mixed mode. Therefore the duty ratio of Q1 and Q2 will be reduced by the controller. The impact of over-current is signified as waveforms and the operation modes at steady states are displayed in Figure12 distinctly. Q1 and Q2 are proportionally turned on in a moment with the same duty cycle D. There are eight operation modes within a period. Every four modes in each half cycle are fairly similar. Thus only the four modes are explained below.



(a) Mode 1: t0 - t1 (resonant mode )



(b) Mode 2: t1-t2 (DAB mode)



(c) Mode 3 : t2-t3 (DAB mode)



(d) Mode t3-t4

#### Figure 6 Equivalent circuit of converter under over current operation.

## Mode 1 [t0-t1]: A-B

In this mode, at t0,  $i_{Ls} = 0$  and  $V_{crl} =$  zero. Equivalent circuit is shown in Figure 6(a). As soon as Q1 and Qr1 work, positive voltage is applied to the resonant tank and  $L_s$  resonates with  $C_{r1}$  and  $C_{r2}$ . Half of the resonant current  $I_{Ls}$  charges  $C_{r1}$  and the remaining passes through the load to discharge  $C_{r2}$ . The operation point travels along the trajectory curve from point A towards point B. The center of operation point is  $(V_{HV_dc}/2n, 0)$ , where n is the turns ratio of the transformer. The radius is the length of O1A, which is  $V_{HV_dc}/2n$ . This functional mode resembles LLC resonant converter and thus referred as resonant mode in our work. Now the derivation are as follows

$$i_{Ls}(t) = \frac{r}{2r} \sin(\omega_r(t-t_0))$$

$$V_{crl}(t) = r \cdot r\cos(\omega_r(t-t_0))$$

$$Where, \omega_r = \frac{1}{\sqrt{L_s(C_{r1}+C_{r2})}}, r = \frac{V_{hv\_dc}}{2n} (6)$$

#### Mode 2 [t1-t2]

B-C.Mode1,referred as the resonant mode is completed when  $V_{Cr1}$  picks up  $V_{LV_dc}$  and  $V_{Cr2}$  is discharged completely. Figure 6(b) is the equivalent circuit of this mode. At t1, the inductor current passes through D4 via  $C_{r1}$  and  $C_{r2}$ , where exactly, the converter shifts to DAB mode. The voltage difference between  $V_{HV_dc}/2n$  and  $V_{LV_dc}$  will energise the current of  $L_s$  to ramp up or down (7):

$$i_{Ls}(t) = I_{Ls\_t1} + \frac{\frac{V_{hv\_dc} - 2nV_{lv\_dc}}{2nL_s} (t-t_1)(7)}{arccos(\frac{V_{hv\_dc} - 2nV_{lv\_dc}}{V_{hv\_dc}})}$$

ωr

Where, t1=

 $I_{Ls_{t1}} = \frac{\sqrt{V_{hv_{dc}}^2 - (V_{hv_{dc}} - 2nV_{hv_{dc}}^2)}}{2nZ_r}$ (8)Our work majorly concentrates on the least condition f heavy load's short circuit. When  $V_{LV_{dc}}$  is almost zero,  $I_{Ls}$  rises up in this mode. The trajectory path travels from point B to C.

#### Mode 3 [t2-t3]: C-D

In this mode, at t2,Q1 is opened. The primary current is transmitted to the body diode of Q2 (Figure 6 (c)). Voltage across  $L_s$  is shifted to negative polarity(Figure 6 (c)).  $I_{Ls}$  (8) decreases linearly, as illustrated in the path from point C to D.

$$i_{Ls} = I_{Ls_{-t2}} - \frac{V_{h\nu_{-dc}} - 2nV_{l\nu_{-dc}}}{2nLs} \quad (t - t_2) \text{ (9)Where, } t_2 = DT_s \text{,}$$

$$I_{Ls_{-t2}} = I_{Ls_{-t1}} + \frac{V_{h\nu_{-dc}} - 2nV_{l\nu_{-dc}}}{2nLs} \quad (t - t_2) \quad (10) \text{Mode 4 [t3-t4]: D}$$

In this mode, at t3,  $I_{Ls}$  is completely zero and the converter is retained in this mode till Q2 is closed. The overlooked factors in this mode are voltage balancing between Cr1 and Cr2, the resonance between the freeloading inductance and capacitors of transformer, semi-conductor devices. Thus we take on that the operation point retains at D. In mode 1, Cr1 and Cr2 equally part the resonant current, while in mode 2 and mode 3, whole  $I_{Ls}$  is consumed by the load. Incorporating the law of capacitor charge balance to  $C_{LV_{dc}}$ , the average output current  $I_o$  can be derived as (38). Using the parameters from Table I, a 3D plot showing the connection between output current  $I_o$ , duty cycle, and  $V_{LV_{dc}}$  under the over current protection scenario is given in Figure 13. When these parameters are reaching towards zero, the output current, on over current condition will decrease. Since the output power is partial, the converter maintains lowV<sub>LV\_dc</sub> by small duty ratio for heavy loads. Figure 7 (a), (b) show the corresponding V-I characteristic curve at 6 kV and 3kV respectively. They infer that the output current can certainly be limited by the converter disregarding of duty cycle maintained close to 0.5. In the interim, further constraint can be realized by decreasing the duty cycle.

$$I_{0=} \frac{\int_{0}^{t_{1}} i_{LS}(t) dt - I_{LS\_t1}}{T_{S}} (t_{2}-t_{1}) + I_{LS\_t2} (t_{3}-t_{1})}{T_{S}} (11)$$
Where,  $t_{3} = DT_{s} + \frac{2nI_{LS\_t2}}{V_{hV\_dc} + 2nV_{IV\_dc}} L_{s}$  (12)

Figure 7I<sub>Output</sub> versus D and  $V_{LV}$ dc ( $V_{HV}$ dc = 6 kV)





Figure 8V<sub>lv\_dc</sub> versus output current

#### 4. Result and Discussion

A simulation model is designed for endorsement of our existing converter. Intending the operation range from 250V to 350V, the normal input range is designed from 320V to 350V and the output voltage is fixed as 200V. The following parameters listed below in the table are enhances the validation of the performance of the converter

Input voltage Vd	250-350V
Output voltage	Vo 200V
Switching frequency	fs 50kHz
Primary winding turns	Np 24turns
Secondary winding turns	Ns 8turns
Magnetizing inductance	Lm 695µH
Leakage inductance	Llk 8.3µH
Clamp capacitor	Cc 11µF
Resonant capacitors	Cr1,Cr2 680nF
Output capacitor	Co 680µ

Table 4.1: Specifications of the converter design

The above said parameters in the table enhance the validation of the performance of the converter. ThePlexim tool is chosen as a best alternative of Matlab Simulink. The existing converter is simulated and PLECS Block set users is enabled for advance modeling of exceptional control of various fields using Simulink library. Each PLECS circuit is signified as separate block in a Simulink model. The user can control the block by transferring signals to unitevarious sources and switching devices. Measurements observed inside the PLECS Circuit block are accessible at the block's outputs. Measurements displayed in a scope are brought under follow-up process in MATLAB andare used to control the system.

The circuit diagram and simulation model of the Hybrid-type converter is shown in Figure 9. When input terminal tracks voltage of 350V, the existing converter is activated by phase-shift control maintaining the constant duty ratio of 0.5. Similarly at 250V, the existing converter is driven by the asymmetrical PWM control with D, 0.61. The regulation is retained in both modes for output voltage  $V_{0}$ .



Figure 9. PWM controlled generating signals of the existing converter

The I/O characteristics exhibit the input voltage  $V_{in}$  around 350 V and the output voltage  $V_{o}$ , approximately as 230 V, which proves the modest operation of the existing converter.



Figure 10Simulation model of the existing converter in the plexim environment



Figure 11I/O characteristics of the existing converter



Figure 12 Trigger signals generated by the existing converter in the phase shifted mode



Figure 13Waveforms representing S1 state.Initiated with ZVS turn-on, the current throughS1starts from zero and ramp with the voltage.



Figure 14waveforms representing S2 state. ZVS is activated and ZCS is deactivated.



Figure 15 Experimental waveforms of the existing converter showing current pressure when  $V_d$  is assigned to 350V.



Figure  $16V_{Output}(V_{o) Vs}Ioutput(I_{o})$  of existing converter







# Figure 18signification of the performance based curve of conventional and proposed converter.

Simulation plan: with a target of succeeding all the qualities, a bidirectional isolated dc-dc converter is deployed. It implements both step up and step down conversion. Theswitching frequency is 40KHZ with D fixed as 0.42.

## **Step up conversion:**



Figure 19 PLEXIM simulation of the projected circuit: step up transformation



Figure 20I<sub>input</sub>VsV<sub>output</sub>

The Input and output voltage outlines are shown distinctly with step up ratio. The input voltage provided is 40V. Step up conversion is done up to 186V.



# Figure 21PWM outline for the proposed converter.

Q1 and Q2 are proportionallyactivated in a swapping period with equal duty cycle.



#### Figure 22 Capacitor voltages Vcr1, Vcr2 and Vcr3 across HV side.



#### Figure 23Capacitor voltages Vc1 and Vc2 acrossLV side.



# Figure 24 Graphic representation of ILS

where,  $i_{Ls}$  is current through the resonant inductor to offer leakage inductance.

#### Step down conversion:



Figure 25 PLEXIM simulation of the projected circuit: step down transformation.



#### Figure 26Input and output voltage outlines with step down ratio.

The input voltage provided is 200V. Step down conversion is done up to 40V.



#### Figure 27 PWM outline for the proposed converter.

Q1 and Q2 are proportionally activated in a swapping period with equal duty cycle.



#### Figure 28Capacitor voltages Vcr1, Vcr2 and Vcr3 across HV side.



#### **Figure 29Input voltage V**<sub>s</sub> Efficiency



Figure 30Capacitor voltages Vc1 and Vc2 across LV side.



Figure 31Graphic representation  $ofi_{Ls}$   $i_{Ls}$  is current through the resonant inductor to offer leakage inductance.



Figure 32Indication of efficiency of the projected circuiton step down state.



Figure 33 representation of Voltage input V<sub>s</sub> voltage output response



Figure 34 Loadcapacity Vs efficiency

## 5. Conclusion

Thus the association of a LLC resonant and dual active bridge converter (DAB) forms bidirectional dcdc converter to compensate moderate voltage request with static resonant frequency. In case of normal load, the converter shots at resonance. Primary side has zero voltage turn on (ZVS) and achieves zero current turn off (ZCS) at secondary. In case of overload, the resonant capacitor voltage is compressed by parallel diode and the converter maintains dual mode of resonant and DAB. The proposed converter is conveyed in terms of strategy scheme of all devices, time domain wave form, dual power usage, efficiency and state trajectory.

High efficiency is accomplished by implying lenient switching techniques on primary switches and rectifier diodes. Thus consistency is improved for every phase including startup and run position by determining the over current disorder. The hybrid operation enables the proposed converter to provide larger phase-shift value with reduced conduction losses. Thus it leads the conventional type. Only limitation is power delivered below the standard level because of duty cycle variation.

## References

- 1. Sabate J.A., Vlatkovic V., Ridley R.B., LeeF.C. and Cho B.H., Design considerations for highvoltage high power full bridge zerovoltageswitching PWM converter, Applied Power Electronics Conference, 1990, pp. 275-284.
- 2. Lee I.O., and Moon G.W., Phase-shifted PWM converter with a wide ZVS range and reduced circulating current, IEEE Transactions on Power Electronics, Feb. 2013, vol. 28, No.2, pp. 908-919.
- 3. Shin Y.S., Hong S.S., Kim D.J., Oh D.S. and Han S.K., A new changeable full bridge dc/dc converter for wide input voltage range, Proceedings of 8th International Conferenceon Power Electronics in ECCE Asia, May 2011, pp. 2328-2335.

- 4. Jain P.K., Kang W., SoinH. and Xi Y., Analysis and design considerations of a load and line independent zero voltage switching full bridge dc/dc converter topology, IEEE Transactions onPower Electronics, Sep. 2002, vol. 17, no .5, pp. 649-657.
- 5. Lee I. O. and Moon G. W., Soft-switching DC/DC converter with a full ZVS range and reduced output filter for high-voltage application, IEEE Transactions on Power Electronics, Jan 2013, vol. 28, no .1, pp. 112-122.
- 6. Yadav G. N. B. and Narasamma N. L., An active soft switched phase shifted full-bridge dc-dc converter : analysis, modeling, design, and implementation, IEEE Transactions onPower Electronics, Sep 2014, Vol. 29 No. 9, pp. 4538-4550.
- 7. Jang Y., JovanovicM.M., and Chang Y.M., A new ZVS-PWM fullbridge converter, IEEE Transactions onPower Electronics, Sep 2003, vol. 18 no. 5, pp. 1122-1129.
- 8. Song T.T.and Huang N., A novel zero-voltage and zero-currentswitching full-bridge PWM converter, IEEE Transactions onPower Electronics, Mar 2005, vol. 20, no. 2, pp. 286-291.
- 9. Huang R. and Mazumder S.K., A soft-switching scheme for an isolated dc/dc converter with pulsating dc output for a three-phase highfrequency link PWM converter, IEEE Transactions onPower Electronics, Oct 2009, vol. 24, no. 10, pp. 2276-2288.
- 10. SeokK.W.and Kwon B.H., An improved zero-voltage and zerocurrent-switching full-bridge PWM converter using a simple resonant circuit, IEEE Transactions on Industrial Electronics, Dec 2001, vol. 48 no. 6, pp. 1205-1209.
- 11. Noue, Shigenori, and Hirofumi Akagi, A bidirectional isolated DC–DC converter as a core circuit of the next-generation medium-voltage power conversion system, IEEE Transactions on Power Electronics, 2007, Vol. 22, No.2, pp. 535-542.
- 12. Fan, Haifeng, and Hui Li., Highfrequency transformer isolated bidirectional DC–DC converter modules with high efficiency over wide load range for 20 kVA solid-state transformer,IEEE Transactions on Power Electronics, 2011, Vol. 26, No.12, pp. 3599-3608.
- 13. GuB., Lai J.S., KeesN. And ZhengC., Hybrid-switching full-bridge dc–dc converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehiclebatterychargers,IEEETransactions on Power Electronics, Mar 2013, vol.28, no.3, pp.1132-1144.
- 14. Lee W.J., KimC.E., Moon G.W., and Han S.K., A new phase-shifted fullbridge converter with voltage doubler type rectifier for high efficiency PDP sustaining power module, IEEE Transactions of Industrial Electronics, Jun 2008, vol. 55 no. 6, pp. 2450-2458.
- 15. Kim E.H.and KwonB.H., Zerovoltage and zero current switching fullbridge converter with secondary resonance, IEEE Transactions of Industrial Electronics, Mar 2010, vol. 57 no. 3, pp. 1017-1025.

#### \*\*\*\*\*